



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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<p>(54) Title: <b>SMART BATTERY DEVICE</b></p>	
<p>(57) Abstract</p> <p>A smart battery device (10) which provides electrical power and which reports predefined battery parameters to an external device having a power management system, includes: at least one rechargeable cell (26) connected to a pair of terminals (31 and 32) to provide electrical power to an external device (28) during a discharge mode, and to receive electrical power during a charge mode, as provided or determined by remote device (28); a data bus for reporting predefined battery identification and charge parameters to the external device; analog devices for generating analog signals representative of battery voltage and current at the terminals, and an analog signal representative of battery temperature at the cell; a hybrid integrated circuit (IC) (32) having a microprocessor (50) for receiving the analog signals and converting them to digital signals representative of battery voltage, current and temperature, and calculating actual charge parameters over time from the digital signals, the calculations including one calculation according to the following algorithm: <math>CAP_{rem} = CAP_{FC} - \sum Id \Delta t - \sum Is \Delta t + \sum ec \Delta t</math> wherein <math>ec</math> is a function of battery current and temperature; and <math>Is</math> is a function of battery temperature and <math>CAP_{FC}</math>. Superimposed on this equation is reset logic, that self corrects the <math>CAP_{FC}</math> with a capacity calculation at each full charge (EOC) and each end of full discharge.</p>	

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SMART BATTERY DEVICE

1

1. Field of the Invention

The present invention relates to generally to the art of rechargeable batteries and more specifically to a smart battery for use in an intelligent device having power management capabilities. The invention is a smart battery apparatus for controlling the operation of rechargeable Nickel Metal Hydride (NiMH) or Nickel Cadmium (NiCad) batteries, and the like, to enable the reporting of accurate information to the intelligent device for power management and charge control specific to the battery's state of charge and chemistry.

2. Description of the Prior Art

The advent of intelligent portable electronic devices such as notebook computers, video cameras, cellular phones has enabled the development of smart rechargeable batteries that can communicate with the intelligent device to provide accurate information on the battery's present state of charge, and how best to recharge the battery to maintain maximum battery life, thus enabling the highest number of charge-discharge cycles. A user of such intelligent portable devices utilizing such smart batteries will not only know how much charge is left in the battery, but battery run time at various rates of power consumption. This enables the user to select a mode of operation that will enable maximum service life on the remaining state of charge and, how long the device will continue to operate.

Prior art rechargeable battery units have been provided with means for generating some desired information to their users, including for instance, a charge monitor and fuel gauge such as that disclosed in U.S. Patent No. 5,315,228 which discloses a method for

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calculating state of charge and reporting run time to  
1 empty to the host computer system.

However, there is a need for a rechargeable  
power unit that will accurately maintain its own state  
of charge information even when nominally fully  
5 discharged such that a user will have instantaneous  
access thereof. Moreover, there is also a need for an  
intelligent rechargeable battery that can provide the  
user with an accurate prediction of its remaining  
operating time at various levels of power consumption.  
10 The user of such an intelligent device, such as a  
portable computer, can thus elect to power down a hard  
disk drive to extend the operation of the portable  
computer for a longer period of time than would had been  
possible at the higher rate of power consumption.

#### 15 SUMMARY OF THE INVENTION

Accordingly, it is an object of the present  
invention to provide a smart battery device for use with  
a rechargeable battery to be installed in a host  
computer that will optimize the performance of the  
20 rechargeable battery throughout its life cycle.

It is another object of the instant invention  
to provide a smart battery device that includes a  
microprocessor for controlling a rechargeable battery  
that performs battery capacity calculations for  
25 communication to a host computer device or a smart  
battery charge device.

It is still another object of the instant  
invention to provide a smart battery device that  
includes a microprocessor for controlling a rechargeable  
30 battery and that provides intelligence in the form of  
present state of charge and battery charge parameters to  
a host device for communication to a smart charger.

It is yet still a further object of the  
1 instant invention to provide a smart battery device that  
includes a microprocessor for controlling a rechargeable  
battery that monitors battery operating parameters such  
as voltage, current, and temperature to thereby enable  
5 either a rapid charging rate or an optimal charging rate  
from any charged state.

Still yet another object of the instant  
invention is to provide a smart battery device that  
includes a microprocessor for controlling a rechargeable  
10 battery that calculates predictive data such as the  
battery's remaining life at the current rate of drain  
and at alternate rates of drain.

It is still a further object of the instant  
invention to provide a smart battery device that is an  
application specific integrated circuit (ASIC) having  
15 analog and digital components.

Furthermore, another object of the present  
invention is to provide a smart battery device that  
includes an analog to digital (A/D) converter for  
20 measuring battery charge parameters such as voltage,  
current, and temperature.

Yet still another object of the present  
invention is to provide a smart battery device having an  
A/D converter with a single positive power supply that  
25 is capable of bipolar operation for converting both  
positive and negative analog signals representing  
battery charge and discharge currents, respectively.

Another object of the instant invention is to  
provide a smart battery device as above wherein the  
analog and digital components of the ASIC comprise CMOS  
30 semiconductor technology designed for improved accuracy,  
and high A/D converter resolution with minimal power  
consumption.

Still another object of the present invention  
1 is to provide a smart battery device having a  
microprocessor such that, when nominally discharged,  
will place itself in a sleep mode with virtually no  
power consumption.

5 Yet a further object of the present invention  
is to provide a smart battery device that includes a  
microprocessor with RAM memory, and comprises means for  
retaining RAM memory contents when the device is in  
sleep mode.

10 Yet still a further object of the invention  
is to provide a smart battery device that comprises  
short circuit protection means for preserving RAM memory  
contents when battery is temporarily short circuited.

Another object of the instant invention is to  
15 provide a smart battery device that includes a ROM  
memory that is manufactured by a process that  
facilitates the programming of ROM in an upper or  
respectively later produced layers.

Yet furthermore, an object of the instant  
20 invention is to provide a smart battery device that  
includes a ROM memory device whereby the programming of  
ROM is effected in a metal mask.

Furthermore, an object of the instant  
invention is to provide a smart battery device having  
25 incorporated therein an error treatment algorithm, for  
taking into account measurement errors, interpolation  
from look-up tables, etc., wherein the errors are  
considered to be a function of time. It is contemplated  
that if a total error is larger than a predetermined  
value, certain operating modes are disabled, and, in  
30 particular, variables are substituted by default values  
to result in a smaller error. In case of displayed  
information, such as LED battery pack display, the error  
can be additionally taken into account, for e.g., a

quantity of: capacity - total error in capacity, may be displayed. If an error that is too big is produced, the end criterion for determining end of charge condition may be changed, for e.g., using  $-dU$  instead of the error influenced criterion.

These and other objects of the present invention are attained with a smart battery device which provides electrical power and which reports predefined battery parameters to an external device having a power management system, wherein the battery includes:

(a) at least one rechargeable cell connected to a pair of terminals to provide electrical power to an external device during a discharge mode and to receive electrical power during a charge mode, as provided or determined by said remote device,

(b) a data bus for reporting predefined battery identification and charge parameters to the external device,

(c) an analog means for generating analog signals representative of battery voltage and current at said terminals, and an analog signal representative of battery temperature at said cell,

(d) a hybrid integrated circuit (IC) having a microprocessor for receiving the analog signals and converting them to digital signals representative of battery voltage, current and temperature, and calculating actual charge parameters over time from said digital signals, said calculations including one calculation according to the following algorithm;

$$CAP_{rem} = CAP_{FC} - \sum I_d \Delta t_d - \sum I_c \Delta t_c + \sum \epsilon_c I_c \Delta t_c$$

wherein  $\epsilon_c$  is a function of battery current and temperature; and  $I_c$  is a function of battery temperature and  $CAP_{FC}$ .

(e) a data memory defined within said hybrid IC for storing said predefined battery identification

and actual charge parameters, even when nominally fully discharged, said charge parameters including at least full charge capacity and remaining capacity,

(f) a bus controller defined within said hybrid IC for sending battery messages to said remote device over said data bus, said messages including said predefined battery identification and said actual charge parameters.

Superimposed on this equation is reset logic, to be explained below, that self corrects the value of  $CAP_{rc}$  with a capacity calculation at each full charge (EOC) and each end of full discharge.

Further benefits and advantages of the invention will become apparent from a consideration of the following detailed description given with reference to the accompanying drawings, which specify and illustrate preferred embodiments of the invention.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagrammatic block diagram of a smart battery device connected to a host computer and battery charging device.

Figure 2(a) is a simplified block diagram of the smart battery device and connector, including a pinout diagram of an Application Specific Integrated Circuit (hybrid IC) used in the present invention.

Figure 2(b) illustrates a simplified block diagram of the hybrid IC 32 that includes the microcontroller of the smart battery device of the instant invention.

Figure 3 is a general flow diagram illustrating the primary functional features of an algorithm and method for controlling the smart battery device of the instant invention.



Figure 4 illustrates a general schematic diagram of the A/D converter 60.

Figure 5(a) illustrates a schematic sketch of dc voltage shifting circuit arrangement.

Figure 5(b) illustrates a second embodiment of the dc voltage shifting circuit arrangement.

Figure 6 is a schematic sketch of the circuit arrangement in the A/D converter 60.

Figure 7 is a phase diagram in the operation of the A/D converter pursuant to Figure 6.

Figure 8(a) illustrates the timing of the operating cycles under normal and sample mode operating conditions.

Figure 8(b) illustrates the approximate time durations for the various measurements per operating cycle.

Figure 9(a) illustrates a schematic sketch of a sample transition arrangement for the ROM included in the smart battery device; and

Figure 9(b) is a schematic sketch of the transistor arrangement of an ROM programmed pursuant to the prior art.

Figure 10 is a detailed schematic of the power-on reset 85 and RAM de-latching circuit 85'.

Figure 11 illustrates a detailed schematic diagram of the comparator wake-up circuit 80.

Figure 12 is a flow diagram illustrating the IUT (current, voltage, and temperature) calculation program 200.

Figures 13(a) and 13(b) are flow diagrams illustrating the sequential processes 151 programmed in the microprocessor for calculating the current capacity and the amount of battery self discharge for the smart battery of the instant invention.

Figure 13(c) illustrates the integration  
1 program 400 for calculating the amount of battery charge  
or discharge flowing into or out of its terminals.

Figures 14(a) through 14(c) are flow diagrams  
illustrating the sequential processes 500 programmed in  
5 the microprocessor for determining battery end  
conditions when the battery is in a capacity increasing  
state.

Figure 14(d) illustrates a flow diagram of the  
learn number of cells program 700.

Figures 15(a) and 15(b) are logic flow  
10 diagrams illustrating the sequential processes 600  
programmed in the microprocessor for determining battery  
end conditions when the battery is in a capacity  
decreasing state.

Figure 16 illustrates a logic flow diagram of  
15 the handle request routine that is invoked when there is  
communication between the smart battery and the host  
computer or battery charger.

Figure 17 illustrates a detailed logic flow  
20 diagram of the write block routine for writing data to  
the smart battery.

Figure 18 illustrates a detailed logic flow  
diagram of the read block routine for reading data from  
the smart battery.

Figures 19 illustrates a flow diagram  
25 describing the logic steps invoked by the smart battery  
system when broadcasting an alarm condition to an  
external device.

Figure 20 illustrates a logic flow diagram  
30 describing the steps invoked by the smart battery system  
when broadcasting a charge condition to a battery  
charger.

Figure 21 illustrates a logic flow diagram describing the steps invoked by the smart battery system when broadcasting a message.

Figure 22(a) is a three-dimensional graphic representation of look up tables that depict predicted residual capacity values as a function of discharging current and temperature.

Figure 22(b) is a three-dimensional graphic representation of look up tables that depict the amount of self-discharge current (vertical axis) as a function of relative battery state of charge and temperature.

Figure 22(c) is a three-dimensional graphic representation of charge efficiency look-up tables showing charge efficiency factors as a function of relative state of charge, charging current, and temperature.

Figure 23 illustrates two voltage versus time graphs, a and b, comparing calculated battery capacity characteristics at various discharging current rates for a six (6) cell battery pack.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The smart battery device of the present invention is intended for use with an intelligent host device such as a portable computer, portable video camera or cellular telephone having a system management bus and a smart charger, or an intelligent host device having a system power manager that can receive and send data over a system management bus.

A representative example of such a system is illustrated in Fig. 1, wherein the smart battery 10 is connected to a power plane 12 to supply and receive electrical energy over the power plane, and a system management bus 14, which is a bi-directional modified

I2C data bus (communication interface) that communicates with a host device 16 which may be a portable computer. The host device 16 may be powered by the smart battery 10, or by the system power supply 18 and a conventional AC source 20. A system power supply or power management system also communicates with a smart charger 22 which may be used to determine the rate and duration of charge sent to the smart battery by the power supply. Smart charger 22 also communicates with the system management bus 14, and may receive a temperature signal representative of battery cell temperature on a separate line feed 24. A detailed functional description of the system management bus 14 (bi-directional modified I2C data bus) can be found in the Intel\Duracell System Management Bus Specification, Rev 0.95, (April 1994).

The system power management system 18 may supply or draw power to/from the smart battery 10 over power plane 12, depending upon the state of charge in smart battery 10, and depending upon the presence or absence of power at AC source 20.

The smart charger 22 may periodically poll the smart battery 10 for charge characteristics, and adjust output to match a smart battery charge request. Optionally, and if selected by the user of the host device, the smart charger 22 can override the smart battery's charge rate request and charge the smart battery at a higher or quick charge rate. The user of the host device does not necessarily need to override the smart battery's request. As will be explained in greater detail below, the smart battery may periodically broadcast the desired charging current, or the smart charger 22 polls the smart battery for a charging current. The host or the charger need not comply with the smart battery's request and can provide a greater or lesser amount of power than requested.

-11-

1 The host device 16 may communicate with the  
smart battery over the system management bus 14 and  
request information from the battery for use in the  
system power management scheme, thereby providing the  
user of the host device with information about the  
5 battery's present state and capabilities. The host  
device 16 will also receive notice of critical events,  
including alarm conditions, remaining capacity below a  
user set threshold value, a remaining run time below a  
user set threshold value, or an end of discharge signal.  
10 The alarm conditions include but are not limited to  
overcharging, overtemperature, a remaining charge  
capacity below a predetermined or user set capacity, or,  
a run time below a predetermined or user set run time  
remaining.

15 As will be hereinafter explained in greater  
detail, the smart battery can report out an  
instantaneous current value being drawn from the  
battery, current values averaged over predetermined time  
intervals, present temperature and present voltage.

20 The smart battery may also report out a number  
of battery status indicators, indicating whether or not  
the battery is charging or discharging, that charging is  
complete, or, that the battery is fully discharged.

25 In addition, it can provide calculated values  
including run time remaining at a present current usage,  
a run time remaining at an average current use, a run  
time remaining at optimal current use, and a predicted  
run time remaining at a host device selected current  
level (discharge rate).

30 The smart battery device 10 is also provided  
with a read-only memory (ROM) that is manufactured to  
contain a set of predefined battery identification  
parameters which may include manufacturer data, cell  
chemistry, design capacity, design voltage, and a unique  
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-12-

device identification number. The predefined battery  
1 identification parameters are available, for either the  
host device or the smart charger, to assist them in the  
selection of optimal usage and charge parameters for the  
smart battery.

5 The smart battery is also capable of  
recommending a desired charge current, reporting a time  
remaining to full charge, a battery capacity available  
at full charge, and the number of times the battery has  
been charged or discharged.

10 The smart battery of the present invention  
utilizes a hybrid integrated chip (IC) containing an  
embedded microprocessor and a novel analog to digital  
converter which receives analog signals from the battery  
and converts them to digital signals representative of  
15 battery voltage, current and temperature. The smart  
battery microprocessor then calculates actual charge  
parameters over time from these digital signals  
according to a predetermined algorithm in which  $CAP_{rem}$  is  
the remaining capacity of the battery which is  
continuously assigned a new value to reflect adjustments  
20 for effective charge, discharge, and self discharge.

The charge delivered to the battery is  
measured, and adjusted by an efficiency factor which is  
a function of current, temperature, and relative state  
of charge. It should be mentioned that the remaining  
25 capacity,  $CAP_{rem}$ , and the relative state of charge, SOC,  
represent the same thing (remaining battery capacity)  
and differ in that relative state of charge is indicated  
as a percentage of the last full charge capacity. The  
charge efficiency is a value determined as a function of  
30 the above variables and may be derived from a look up  
table, hereinafter described with respect to Figure  
22(c), or calculated from a formula which provides a  
stepwise approximation of charge efficiency behavior,

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depending upon current, temperature and state of charge.

1 It is understood that the charge efficiency factor can  
be obtained from a response equation or interpolation  
between several different values stored in memory.

5 Likewise, the remaining battery capacity  $CAP_{rem}$   
is decremented by the measured discharge rate over time.  
A predictive model of residual capacities determines  
expected  $CAP_{rem}$  for a present current and temperature.

10 This predictive model may also estimate when the battery  
voltage will drop to a predetermined cut-off voltage for  
the present rate of discharge. This residual capacity  
model may be calculated from a formula or obtained from  
a look up table, which includes values of residual  
capacities as a function of discharge current and  
temperature.

15 Finally,  $CAP_{rem}$  is also adjusted by subtracting  
self discharge. Self discharge is calculated as a  
function of temperature and state of charge, and is  
always subtracted from  $CAP_{rem}$ , regardless of whether the  
battery is discharging or being charged. Self discharge  
20 may be derived from a look up table of empirical models  
of identical cell chemistry that predict self discharge  
as a function of temperature and state of charge, or may  
be calculated by the microprocessor.

As will be hereinafter explained in greater  
detail,  $CAP_{rc}$  is a learned value which is self correcting  
25 because of reset logic incorporated in the capacity  
algorithm. The capacity algorithm takes actions on four  
types of end of charge (EOC) signals, including a  
negative voltage slope at a full charge voltage, a  
temperature rise that exceeds a predetermined rate, or a  
30 calculated state of charge that is equivalent to a value  
of 100% to 150% of the previous  $CAP_{rc}$  value, if an  
optimal charging current has been used, or a high  
temperature limit value. When one of the first three of

the above four types of conditions is encountered, the  
1 reset logic resets  $CAP_{rc}$  to the previous  $CAP_{rc}$  value,  
sets a fully charged status flag, and, signals the host  
device and charger to terminate charge. If the high  
temperature limit is reached, only a signal to terminate  
charge is invoked.

5 The charge algorithm terminates its  
integration of the present discharge state when it  
reacts to an end of discharge (EOD) signal between 0.9  
volts/cell and 1.1 volts/cell and preferably 1.02 volts  
10 per cell. At that point it resets  $CAP_{rc}$  to a new  
learned value of residual capacity, as determined from  
the integration of the discharge current, as a function  
of discharge current and temperature.

As will be hereinafter explained in greater  
15 detail, the reset logic will reset  $CAP_{rc}$  as a function of  
which EOD signal was acted on. Thus a new  $CAP_{rc}$  value  
for the smart battery's actual capacity is learned after  
each full discharge cycle, as a function of the last  
fully integrated battery discharge cycle. The smart  
20 battery 10 of the present invention is thus able to self  
correct  $CAP_{rc}$  within one full cycle to readjust its  
capacity at each EOC and EOD, and effectively relearn  
full battery capacity within a single cycle, even if all  
prior battery history has been extinguished by virtue of  
25 a catastrophic memory failure. The smart battery of the  
present invention is therefore able to accurately  
predict actual capacity, and typically is able to  
correctly predict the remaining run time to empty within  
a few minutes for a 2400 mAh battery.

30 Smart battery 10 of the present invention is  
more fully illustrated in Figure 2(a) which is a  
simplified block diagram of the smart battery, an  
advanced design multi-pin connector, and a battery  
module 28 which includes a pinout diagram of the hybrid



ASIC 32 used in the present invention. As illustrated in Figure 2(a), the smart battery device 10 includes a plurality of rechargeable cells generally indicated at 26 which may be Nickel Metal Hydride (NiMH) or Nickel Cadmium (NiCad) cells.

For the purposes of an illustrative but not limiting example, in the following specification, 6 NiMH cells having a nominal 2400 mAh capacity, will be assumed. Such an arrangement of cells is particularly appropriate for powering a portable computer.

A suitable advanced design multi-pin battery connector 30 is used to connect the smart battery to a host device 16 or power supply 18, as previously described with respect to Figure 1. The multi-pin connector 30 includes a positive power supply terminal 31 which is connected to the positive terminal of the first cell, and a negative power supply terminal 33 which is connected to the negative terminal of the last cell. A plurality of rechargeable cells may be connected in series therebetween as illustrated in Figure 2(a).

The smart battery module 28 includes a hybrid IC 32 containing a microprocessor 50 (Figure 2(b)) and a plurality of sensor means for generating analog signals representative of battery voltage, current and temperature. The module also includes a series of four (4) LEDs 34 driven by an LED drive circuit 53 and a switch 35 which may be manually actuated by an end user to determine the state of charge in the battery even when the battery module has been removed from the host device 16. The LEDs 34 may be used to represent a relative state of charge (SOC) in a logic scheme as follows: if the state of charge is greater than 75% (or less than 100%) then all 4 LEDs are illuminated; if the SOC is from 50% to 75%, then 3 LEDs are illuminated; if

-16-

1 SOC is from 25% to 50%, then 2 LEDS are illuminated; if  
SOC is from 10% to 25%, then 1 LED is illuminated, and  
if SOC is less than 10%, a single LED is flashing. As  
mentioned above, relative SOC is remaining capacity  
relative to last full capacity.

5 As shown in Figures 2(a) and 2(b), the hybrid  
ASIC 32 also includes an external crystal 36 operating  
at a fixed frequency which is used as a time base for  
integration of battery current over time, and to ensure  
stable start up after a prolonged standby period when  
10 power is reapplied to the smart battery 10. The smart  
battery of the present invention utilizes two separate  
oscillators, a low power RC oscillator 48 formed within  
the hybrid IC 32 and used as an operating clock for the  
hybrid IC and the A/D converter 60 therein, and, the  
15 external crystal 36. As will be hereinafter described  
in greater detail, the external crystal 36 is used to  
restart the measurement period after each predetermined  
interval to provide for accurate measurements and  
integration of battery conditions, regardless of battery  
20 temperature, which can adversely affect the accuracy of  
the internal oscillator. The frequency value of  
external crystal 36 may range from 10kHz to 66 kHz,  
preferably at 32 kHz and the frequency value of  
oscillator 48 may range from 450 kHz to 460 kHz.

25 The hybrid IC 32 includes a MIKRON GmbH low  
cost, high performance, CMOS 8 bit microcontroller ( $\mu$ P)  
50 with an advanced RISC architecture. A reduced set of  
32 instructions that are all single cycle instructions  
(except for program branches which are two cycles), and  
a Harvard architecture scheme achieves a high level of  
30 performance with minimal power drain. The  
microprocessor operates at a clock input anywhere from  
DC to 10 MHz with 12 bit wide instructions and 8 bit  
wide data path. A free programmable Counter/Timer

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circuitry is provided as well as a free programmable Watchdogtimer. Additionally, the microprocessor is addressable in direct, indirect, and relative addressing modes. The microprocessor 50 is commercially available from Mikron GmbH, located at Breslauer Straße 1-3, D-85386, Echting, Germany, and is available in the U.S.A. through MICROCHIP Technology, Inc., Chandler, U.S.A.

The hybrid IC 32 also includes a plurality of analog circuits which are used, in combination with external analog sensors, to generate digital signals representative of battery voltage, current and temperature as will be hereinafter explained.

For example, as shown in Figure 2(a) battery voltage is obtained from a voltage divider circuit which includes R1 and R2 which are internally switched by a NMOS transistor within the hybrid IC 32 to provide voltage measurement during a small portion of each measurement interval, thereby minimizing current drain on the battery cells 26.

The measurement of battery temperature is accomplished with an NTC-thermistor, illustrated as  $R_{NTC1}$  in Figure 2(a), which varies resistance as its temperature varies. A resistor R3 is connected in series to form a voltage divider circuit between  $V_{ASS}$ , (negative analog power supply voltage)  $V_{TEMP}$ , (the temperature voltage input) and  $V_{REFT}$ , which is a reference voltage applied to the thermistor/resistor string by the hybrid ASIC 32 at pin  $V_{REFT}$ . The temperature voltage input is measured at  $V_{TEMP}$  according to the following formula:

$$V_{TEMP} = \frac{R3}{R3 + R_{NTC1}} \times V_{REFT}$$

wherein the NTC1 value may be 10 kohms at 25° C and varies with temperature. If desired, a look-up table with a plurality of temperature values and a plurality

of  $V_{TDP}$  values may be defined to calculate the battery temperature, and between these values, the temperature is linearly interpolated by the microprocessor within IC 32.

The measurement of battery current is measured through a shunt resistor, illustrated in Figure 2(a) as  $R_{shunt}$ , that is connected in series with the battery cells and negative terminal 33 of cell pack 26. The shunt resistor is of small value, but may range anywhere from 1 mohm to 200 mohms depending on the number of cells and expected usage of the battery. The voltage drop across the shunt is sensed between  $V_{SHUNT}$ , the shunt resistor positive input pin of ASIC 32, and  $V_{ASS}$ , the negative analog power supply voltage.

As shown in Figure 2(b), whenever the analog signals representing battery voltage, current, and temperature are obtained, they are input into an ASIC multiplexor or switching network 55 which enables only one analog signal at a time to be input to the A/D converter 60 for digital conversion. The switching network acts in conjunction with digital logic circuitry for informing the A/D converter, via line 55', shown in Figure 2(b), of the amount of integration cycles to perform depending upon the type of measurement to be converted. For instance, more integration cycles are needed when making a current measurement conversion to ensure a higher bit resolution as compared to when a voltage or temperature measurement is being converted, as will be explained in further detail below with respect to Figure 8(a).

A general schematic diagram of the A/D converter 60 is shown in Figure 4. In the preferred embodiment, the A/D converter 60 is a bipolar, high resolution, incremental sigma-delta converter and consists of three parts: a bandgap reference circuit 62

which provides a preset analog voltage which is used as an analog ground for the A/D; a voltage divider network 64 which divides the present voltage to the analog voltages which are used as the full-scale voltage for the A/D; and, a sigma delta circuit 66 for converting the analog signal to a digital word output at line 69. A/D control circuit 68 having a clock input from the IC oscillator, provides the control for the sigma delta converter which has a different degree of resolution depending on the type of measurement. For instance, in one embodiment of the invention, the A/D converter was configured as having a resolution of 13 bits and a conversion time ranging from 300 to 400 msec for current measurements, and, was configured as having a resolution of 10 bits and a conversion time ranging from 30 to 60 msec for voltage and temperature measurements. The timing diagram for the voltage, current, and temperature measurements in each operating cycle is illustrated as 58a in the timing of operating cycles diagram of Figure 8(a), as explained below.

In one embodiment of the invention, the voltage divider circuit 64 of the A/D converter divides the preset bandgap reference voltage into the following full scale voltages; a 150 mV signal used as the full scale voltage for the battery current measurement; 150 mV, 250 mV, or 350 mV signals used as the full-scale voltage for the battery pack voltage measurement and dependent upon the number of battery cells; and 150 mV used as the full-scale voltage for the battery temperature measurement. These values are illustrative and may vary as battery design varies.

The A/D converter of the smart battery device utilizes a sigma-delta converter circuit 66 as explained above in view of Figures 4 and 6. Details of the sigma-delta converter circuit 66 capable of bipolar conversion

are explained hereinbelow in view of Figures 5(a), 5(b) and Figures 6 and 7. Figure 6 particularly illustrates a switching capacitor network for receiving positive and negative voltage values, indicated as  $V_{IN}$  in Figure 6 for input into an integrator circuit 88 and comparator circuit 89 for output into control and logic circuit 68. In the reference, Jacques Robert et al., (1987) "A 16-bit Low-Voltage CMOS A/D Converter", IEEE Journal of Solid-State Circuits, Vol. sc-22, No. 2, 157-159, an incremental (integrating) sigma-delta converter implementing 4- $\mu$ m CMOS, switched capacitor technology similar to that implemented in the A/D converter of the smart battery device is disclosed. What is described in the reference is a simplified, unipolar A/D converter that is largely insensitive to variations in clock frequency and clock waveforms due to the fact that all signals are represented by charges, rather than currents, as in the switched capacitor integrator that forms the core of the converter.

In the prior art, to measure positive and negative input voltages, a negative power supply is necessary in addition to the positive voltage supply. Thus, where it is desired to measure negative voltages (or currents) such as smart battery discharging current, external components (such as inverters) and circuitry that consume extra power are required, and the prospect of utilizing such circuitry for the low power application such as needed in the smart battery device of the instant invention, is diminished. Instead, to overcome this drawback, the A/D converter 60 of the instant invention does not utilize a negative voltage power supply, but makes use of an available on-chip A/D bandgap reference voltage "AGND" to be used as a virtual ground. The concept of utilizing a "virtual ground" is based on the fact that a voltage stored on a capacitor

can be transferred to another d.c. voltage reference point using analog switches with virtually no loss of charge.

In Figure 5(a) there is represented a first embodiment of the dc voltage shifting circuit arrangement, consisting of three switches S1 through S3, and four connectors A1 through A4 and a capacitor C1 (with the capacitance C1). The connectors A1, through respectively A4 are at the potentials  $\phi_1$  through respectively  $\phi_4$ . As shown in Figure 5(a), the switch S1, and the combination of parallel-connected switches S2 and S3 are connected to opposite terminals of the capacitor C1.

In the following there is described the operation of the inventive circuit arrangement. At the beginning, the switches S1 and S2 are closed and the switch S3 is open. The capacitor charges itself up due to the voltage differential  $\phi_1 - \phi_2$  and stores a charge  $C1 \times (\phi_1 - \phi_2)$ .

In the next step of the inventive process, the switches S1 and S2 are opened and one pole of the capacitor is connected through switch S3 with a potential  $\phi_3$ . Present at the capacitor C1 is now a voltage  $\phi_3 + (\phi_1 - \phi_2)$  which can be tapped off through connection with the connectors A3 and A4 which lie on the potentials  $\phi_3$  and  $\phi_4$ .

In Figure 5(b) there is now represented a further embodiment of the dc voltage shifting circuit whereby an additional switch S4 is provided which, when open, prevents the presence of a potential  $\phi_1$  at the tapping off of the voltage  $\phi_3 + (\phi_1 - \phi_2)$  present at the connectors A3 and A4, when switch S1 is closed.

In Figure 6 there is illustrated the schematic circuit diagram of the inventive circuit arrangement in a switched capacitor A/D converter. The A/D converter

66 possesses an operational amplifier 88 which is  
utilized as an integrator, and an operational amplifier  
89 which is utilized as a comparator. The non-inverted  
input of the comparator 89 by means of the line 91  
stands in connection with the output of the integrator  
88. The inverted input of the comparator 89 and the  
non-inverted input of the integrator 88, are connected  
with a reference potential AGND, (analog ground = 1.25  
volt). The output of the comparator 89 is "high", in  
the event that the output voltage of the integrator 88  
is higher than the reference voltage AGND and "low" in  
the event that the output voltage of the integrator 88  
is lower than the reference voltage AGND. By means of  
the lines L1, L2, L3 and L4, the integrator 88 or, in  
essence, the inverted input and the output of integrator  
88 have connected in parallel therewith a capacitor C2  
with a capacitance C2. The capacitor C2 has a switch SR  
connected in parallel therewith through lines L1 and L5,  
which can effectuate a discharge of the capacitor C2.  
Through a line L6, the inverted input of the integrator  
88 stands in connection, by means of a switch S5 and a  
line L7, with a capacitor C1 having the capacitance C1.  
A line L8 connects the line L7 through a switch SI and  
the line L4 with the output of the integrator 88. The  
line L9 connects the pole of the capacitor C1 facing  
towards the integrator 88 in Figure 6 with a line L10,  
which stands in connection through the line L11, L12 and  
respectively L13, with the switches S4, S7 and,  
respectively S6. Connected to the other pole of the  
capacitor C1 is a line L14, which is connected through  
the switch S3 with the reference voltage AGND = 1.25  
volt. A line L15 stands in connection with line L14 and  
connects through the lines L16, L17, and respectively  
L18, the pole of the capacitor C1, which faces away from  
the integrator 88 in Figure 6, with the switches S2, S1,



and respectively, S8. The internal mass of the chips  $V_{..}$   
= 0 volt stands through the line L19 and, respectively,  
1 L20, in connection with the switches S8, respectively,  
S6. In this matter, through suitable opening and  
closing of the switches S8 and S6, the voltage  $V_{..}$  can be  
5 applied to both poles of the capacitor C1. The input  
voltage  $V_{IN}$  which is to be digitized stands in  
connection with the switches S1 and, respectively, S7,  
through lines L21 and, respectively, L22. In this  
manner, through suitable opening and closing of the  
10 switches S1 and S7, the input voltage  $V_{IN}$  can be applied  
to either of the two poles of the capacitor C1. The  
reference voltage  $V_{REF}$  which determines the resolution  
of the A/D converter is connected through lines L23 and,  
respectively, L24 with the switch S2 and, respectively,  
15 S4. In this manner, the reference voltage  $V_{REF}$ , which,  
for example, consists of 150 milli-volt, can be applied  
to one of the two poles of the capacitor C1. The  
switches S1, ..., S8, SR and SI are preferably CMOS  
switches, especially CMOS transmission gates. The  
20 connection of the input voltage  $V_{IN}$ , the reference  
voltage  $V_{REF}$  and the mass  $V_{..}$  with the input capacitor C1  
of the A/D converter is known in the technology.  
Inventively there is connected through the switch S3 a  
reference voltage AGND = 1.25 volt ( $*V_{..}$  = 0 volt) to the  
input capacitor C1. Similarly, through the inventive  
25 circuit there is facilitated that  $V_{IN}$ ,  $V_{REF}$  and AGND can  
be applied to both sides of the input capacitor C1,  
which presently causes a charging up at different  
polarity of the capacitor C1.

30 In Figure 7, there is illustrated the  
operation of the A/D converter in a phase diagram.  
Thereby, S1 through S8, SR and SI designate the switches  
of the A/D converter 66 pursuant to Figure 6, and CK is

the pulse signal of the comparator 89 in Figure 7. CK' represents a further tapped-off pulse signal.

In the diagram, the switch conditions fluctuate between 0 and 1, whereby 1 signifies that the switch is closed, whereas 0 stands for the opened switch. The operation of the A/D converter can be divided into four phases which are designated with I, II, III and IV whereby I designates a RESET or resetting phase; II an integration phase, III and inverting phase and IV an integration phase of the input voltage of reverse polarity or sign. The cycle is more finely subdivided into steps i, --- xiv. As shown as step i in Figure 7, during the reset phase I, only the switch SR is closed, whereas all other switches are opened. This causes a discharge of the capacitor C2. At the beginning of phase II, as indicated as step ii, in Figure 7 the switches S1 and S6 are closed, whereas all remaining switches remain further open. This causes a charging up of the capacitor to a charge  $\Delta Q = C1 \times (V_{IN} - V_{ref}) = C1 \times V_{IN}$ . In step iii, the switches S3 and S5 are closed, whereas all other switches remain open. One pole of the capacitor is now set to the potential AGND, whereas the other pole of the capacitor C1, through closing of the switch S5, stands in connection with the capacitor C2. There now takes place a charge transfer from the capacitor C1 to the capacitor C2. Inasmuch as the integrator of 88 resultingly causes the two input potentials to be equalized, there is present at the output 91 of the integrator 88 the output voltage  $V_{out}$  equal  $-(C1/C2) \times V_{IN} + AGND$ . In step iv all switches are opened and the comparator pulse CK is 1, meaning, the comparator 89 carries out a comparison between  $V_{out}$  and AGND. Upon the result of this comparison there now depends the further cycle. The representation of the switch conditions in step v must be understood in the

following manner: In step v the switches S2 through S8  
are not closed, but the switches S2 and S6 are closed,  
and S1, S3, S4, S5, S7, SR and SI are open, in the event  
that the output of the comparator is 0, in effect "low",  
while the switches S4 and S8 are closed and S1, S2, S3,  
S5, S6, S7, SR and SI are open when the output of the  
comparator is 1, meaning, "high", and in other instances  
remain open. When the output of the comparator is 0,  
meaning the output voltage  $V_{out}$  is lower than AGND, then  
the switches S2 and S6 are closed. At the capacitor C1  
there are now present  $V_{REF}$  and  $V_{SS}$ . In the instance in  
which the output of the comparator is 1, meaning,  $V_{out}$  is  
higher than AGND, then the switches S4 and S8 are  
closed, whereby similarly  $V_{SS}$  and  $V_{REF}$  are present at the  
two poles of the capacitor C1, but with the reverse sign  
or polarity than in the instance in which the output of  
the comparator is 0. In step v, the switches S1, SR and  
SI are opened, and in step vi, the switches S3 and S5  
are closed (compare step iii) which causes that the  
capacitor C1 and C2 to be interconnected. As in step  
iii, voltage AGND is applied to one pole of the  
capacitor C1. There again, in turn takes place a charge  
transfer between the capacitors C1 and C2, as result of  
which a voltage  $-(C1/C2) \times V_{REF} + AGND$  is added to or,  
respectively, subtracted from that of the output voltage  
of the integrator 88, in accordance with the result of  
the comparison by the comparator in step iv. During the  
steps i through vi of phase II there is processed an  
input voltage which is phase shifted with respect to  
AGND, with a reference voltage which is shifted relative  
to AGND. Similarly, at the non-inverted input of the  
integrator 88 and the inverted input of the comparator  
89 there lies AGND, which causes that the output voltage  
is referenced to AGND and causes a comparison by the

comparator 89 not with  $V_{..} = 0$  voltage, but with AGND = 1.25 volt.

1 In the following there is now discussed phase  
III consisting of steps vii to ix. In this phase, a  
sign or polarity reversal is implemented for the output  
voltage  $V_{out}$  of the integrator 88 with reference to AGND.  
5 During the entire phase III the switch S3 is closed.  
The closure of the switch S3 during the phase III causes  
the voltage AGND to be applied to one pole of the  
capacitor C1, as a result of which the voltage  $V_{out}$  is  
also inverted with regard to AGND and not with regard to  
10  $V_{..} = 0$ , as in the known A/D converters. In step vii  
there is now closed the switch S1, whereas all remaining  
switches are open, except switch S3. This causes that  
the voltage  $V_{out}$  is temporarily in the capacitor C1, such  
that in step viii all switches are opened except switch  
15 SR. The switch SR is in effect closed, which causes a  
discharge of the capacitor C2. In the step ix the  
switch S5 is closed additionally to switch S3, while all  
remaining switches are opened. This causes that the  
negative voltage which is phase shifted at AGND is  
20 present at the output of the integrator 88. The  
negative sign is obtained, as previously through the  
charge transfer from the capacitor C1 to the capacitor  
C2. In step x of Phase IV, the switches S7 and S8 are  
closed, whereas all remaining switches are opened.  
25 Compared with the step ii the input voltage  $V_{in}$  is  
present with a reverse polarity at the capacitor C1.  
This causes a change in the sign of the integration of  
the input voltage, which is also well recognizable in  
Figure 6 of the above mentioned publication of Jacques  
30 Robert et al. The steps xi through xiv correspond with  
the steps iii through vi, meaning, there is implemented  
an integration of the input voltage (only due to step x  
with a reverse sign of  $V_{in}$ ), and in accordance with the

1 result from the comparator 89 in step xii  $V_{REF}$  is added  
or, respectively, subtracted after the integration (in  
case  $C1 = C2$ ). For a 14-bit A/D-converter, after  
implementing of step i there is carried out phase II  
[ $2^{14}-2$  (for the phases I, and III)]:2 = 8191 times), as  
5 well as phase IV. The output of the comparator is  
connected to a up/down counter, which each time, in  
accordance as to whether  $V_{REF}$  is added or subtracted,  
increases or lowers its count condition by 1. The  
result of the counter is then a 14-bit representation of  
10 the ratio of  $V_{IN}$  to  $V_{REF}$ . The phases III and IV are  
necessary since through the integration with reverse  
signs of  $V_{IN}$  offset errors encountered in, for example  
the operational amplifiers, are reported or,  
respectively eliminated.

15 The multi-pin connector 30 includes two pins  
for the system management bus interface 75, which  
include a serial clock I/O line 38 and a bidirectional  
serial data I/O line 40. These lines are connected to  
the SMBCLK and SMBD data pins, respectively, of the  
20 hybrid IC 32. As explained generally above, and, in  
greater detail below, the smart battery module 28  
communicates with the host device 16 and the smart  
charger 22 over the system management bus and data line  
40 to communicate both stored battery parameters and  
calculated battery parameters.

25 The smart battery 10 also includes a separate  
thermistor  $R_{NTC2}$  which is connected across the negative  
terminal of multi-pin connector 30 and a temperature or  
thermistor line 42. Thermistor  $R_{NTC2}$  may be used  
independently by the smart charger 22 to determine  
30 battery temperature, in a manner similar to that  
previously described with respect to  $R_{NTC1}$ .

A positive digital power supply voltage is  
obtained from the plurality of rechargeable battery

cells 44, and supplied to the hybrid IC through pin  $V_{DD}$  as the positive power supply voltage for the chip. It should be understood that the supply voltage for the hybrid IC does not necessarily have to be obtained at the battery midpoint 46, but should be obtained at a point from the battery cells in order to receive a voltage of approximately 3 to 4.8 volts, i.e., the equivalent voltage of three (3) cells. As will be hereinafter explained in greater detail, the use of a battery midpoint for the positive voltage supply enables the hybrid IC to remain powered even when the battery is accidentally shorted and removed from terminals 31-33, and enables the A/D converter 60 to determine whether the battery is discharging or being charged as will hereinafter be explained in greater detail. Suitable fuse elements (one of which is shown in Figure 2(a)), and a positive temperature coefficient (PTC) elements (one of which is shown in Figure 2(a)), are provided in series with the battery pack cells to protect the battery from very high current and excessive temperatures caused by a temporary short circuit across the battery terminals or other thermal event.

As shown in Figure 2(b), the hybrid IC 32 further includes RAM memory 65 which can store up to 128 8-bit registers for communication of calculated battery parameters, and a ROM memory 67 for storing look-up table values utilized in the battery capacity calculation algorithm (explained in detail below). The exact amount of RAM, ROM, and program ROM memory is a design choice, and these values change as the ratio between calculated and preset parameters vary.

As shown in Figure 2(a), the addition of capacitor C4 acts as a buffer to maintain the integrity of the RAM memory contents in the case of a battery short-circuit or temporary power loss. Preferably, the

capacitor C4 is connected to the negative analog voltage supply terminal, and its value is chosen to ensure that a source of supply voltage is supplied to the embedded memory (RAM) for a time dependent upon the RAM leakage current. In the preferred embodiment, the power to RAM memory is unlatched if a temporary short circuit condition exists. However, capacitor C4 preferably of capacity 330 nF, provides a source voltage to the RAM for a period of time necessary for the PTC element to ramp to a high resistance value. The PTC element will create a high impedance between battery terminals when a short circuit across the battery pack terminals creates a high circuit drain.

The hybrid IC 32 further includes up to 4 kbytes of additional ROM memory 70 for addressing and storing the various algorithms, subroutines, manufacturer data, and data constants utilized by the smart battery module for calculating the battery capacity, sending messages such as alarms and battery charger control commands etc., and handling message requests from external devices.

The programmable ROM generator is implemented by means of a metal mask (not shown) as opposed to conventional ROM generation by means of diffusion masking. In accordance with the information which was to be permanently stored, transistors were generated in a matrix arrangement through diffusion, whereby the information was coded in the plane through the distribution of the transistors in the diffusion step. Thus, the ROM generator generates in effect, a ROM matrix, whereby the presence or respective absence of an MOS transistor stands for a logic "0" respectively "1." A disadvantage of a ROM matrix with the programmable level of diffusion is that the diffusion process, which is incorporated as one of the first steps of a CMOS

process, can not be changed when there is a change in ROM contents, thus, rendering impossible the production of wafer stock for a particular type of ROM.

By contrast, the advantage of a ROM matrix programmable in a metal layer is that wafer stock with the same basic layers up to the metal may be fabricated. Thus, a microprocessor family with different ROM contents can be realized with low cost and fast turn around time. Additionally, the pre-manufacture of a portion of the ROM with the flexibility of programming in application specific information in the upper or respectively later produced layers, is possible.

The hybrid IC chip itself may comprise thirteen or fourteen layers, with the 9<sup>th</sup> or 10<sup>th</sup> layer (i.e. one of the upper layers) being a layer of metal, wherein the distribution of the metal is characteristic for the storing contents of the ROM. Thus, in the hybrid IC ROM manufacturing process, nine (9) layers are grown and the next four ROM programming layers are grown dependent upon the customer's particular needs (i.e., special properties of the battery pack).

Figure 9(a) shows a ROM matrix with the metal layer as a programmable layer. A MOS transistor, e.g. 71(a) for the matrix is always present on the matrix and will either serve as a logical "0" or "1". Specifically, Figure 9(a) schematically illustrates the ROM 67 of the smart battery device that is programmed according to the unique process as follows: The represented ROM matrix consists of eight word lines 67a and indicated as WZ0, ..., WZ7 and 8 spaces 67b and indicated as SPO, ..., SP8, whereby the spaces SP1, SP3, SP5, SP7 connect with a virtual ground line 73. At each location of the matrix, there is produced a transistor in the diffusion step, three transistors 71a, 71b, and 87 of the matrix are shown in Figure 9(a). For



-31-

the programming of a logic "0," in a respective word line, the drain or respective source electrodes of a transistor are connected to a metal mask with the corresponding source or respectively drain electrodes of the joining transistors or the joining transistor. The drain or respective source electrodes of such a transistor are connected with the gap lines or, respectively, the virtual ground lines 73. Transistor 71a in word WZ7, as shown in Figure 9(a), is programmed for a logic "0" as its drain terminal is connected with the source terminal of connecting MOS Transistor 87 which is tied to virtual ground line SP7.

Logic "1" in contrast therewith is probed in, in that the drain or respectively source electrodes are connected to a common line, preferably, as can be ascertained from Figure 9(a), to a gap line SP0, SP2, SP4, SP6, SP8. Thereby, the transistors, such as the transistor 71b of word WZ0 as shown in Figure 9(a), are short circuited.

The connections of the transistors are thus initially determined with the application of the metal mask. In the usual manner two (through contacting) metal masks are applied on the ROM. It should be understood that in this instance preferably the lower of the two metal masks, meaning the mask which is located closer to the transistors, is employed for the short circuiting and the connection of the applicable transistors. Inasmuch as the transistors are short circuited, this does not influence the operation of the metal mask which is employed for the contacting. Since this metal mask is usually one of the uppermost layers, for example the tenth of about 14 layers, the inventive ROM can be pre-manufactured up to the ninth layer and then programmed and manufactured in accordance with the application.

-32-

In Figure 9(b) there is illustrated a usual programmed ROM. It can be ascertained from Figure 9(b) that the transistors, which are short circuited in Figure 9(a), are in any event not produced in the diffusion mask. As shown in Figure 9(b), the transistor 71c which is not present corresponds to a short circuited transistor 71b in the metal mask pursuant to the process described above.

Each of the algorithms, subroutines, manufacturer data, and data constants stored in ROM and utilized by the smart battery module for calculating the battery capacity, etc. as mentioned above, will now be explained in further detail below. Further details of the smart battery algorithm for reporting battery parameters to an external device is found in applicant's co-pending patent application U.S. Serial No. 08/318,004 assigned to the assignee of the instant invention and the disclosure of which is incorporated by reference herein.

As shown in Figure 3, the battery operating system 10' will first perform an initialization routine 100 that is initiated upon system power up, enabled by a power ON signal/reset impulse signal 11, or, enabled by a wakeup from STANDBY signal 13 which is generated after the microprocessor has determined that it should exit the standby mode. As shown in Figures 2(b) and Figure 10, the hybrid IC 32 is provided with a power-on reset circuit 85 which generates a reset impulse signal 11 to activate the external crystal oscillator 36 and reset the system every time the power supply voltage is applied to the ASIC. Specifically, this reset impulse initiates the start of the external crystal oscillator 36 to provide the precise triggering of the internal 450 kHz oscillator for providing the time base for the hybrid IC components. The threshold of this circuit is

35

between 1.2 V and 1.6 V depending upon the type of transistors used in the circuit of Figure 10.

1 More specifically, as illustrated in Figure 10, the power-on reset circuit 85 is provided with a transistor network comprising n- and p- channel transistors that are tied to hybrid IC voltage supply  $V_{DD}$ . When  $V_{DD}$  is sensed as dropping between 1.6V to 2.0V, or, in the case of battery short circuit 0.0 V, the transistors of circuit 85 generate a RAM memory de-latching signal 79 which turns off PMOS- transistor 85, and effectively de-latches RAM memory 65. As mentioned above, the voltage on buffer capacitor C4 will keep RAM memory contents alive for period dependant upon RAM leakage current.

After a power on/reset signal 11 is received, or, after the sleep mode is exited, the system is placed in a standby mode 23 (Figure 3) until it is triggered by trigger signal 17 generated by the external oscillator 36 which provides the trigger for the system operations (capacity calculation) every 500 msec, or, is awakened by a bus request signal 15 as will be explained in further detail below. In the battery "standby" mode, the microprocessor is in an idle state until the operating cycle trigger 17 or external bus request signal 15 is received.

#### 25 Initialization of algorithm variables

The initialization routine, which is described and shown (in Figure 4) of the above-mentioned, co-pending patent application (USSN 08/318,004), is conducted at the virginal start of the system. The initialization routine functions to clear all values to be stored in the system RAM and to assign all system default values. Preferably, many of the default values

are constant values and are available in case of an emergency situation wherein all RAM memory has been lost while the system was in the STANDBY mode.

On power-on-reset as well as on a wakeup from the STANDBY mode of the chip (explained below), the program is started at an initial memory address. A "checksum" test is conducted for checking whether the RAM memory is valid whereby the capacity calculation is continued, or, whether the emergency mode (which uses ROM defaults) will be activated. Such an instance occurs when the chip switches into the STANDBY mode at low battery voltage and then back into the ON mode when the battery is to be recharged.

If the "checksum" test fails, the  $\mu P$  will first clear all RAM banks completely, and, as consequence an internally generated CALIBRATED flag will be cleared and the number of cells of the battery pack has to be learned, a process to be explained in greater detail below. Next, the default values (described below) are transferred from ROM to RAM. To prevent exceptions in the capacity calculations to be described hereinbelow, it is imperative that variables do not have undefined values. This enables the algorithm to work in a catastrophic emergency mode in the event that all RAM memory has been lost. The default values of critical variables may then be substituted by correct values when the battery system is reformatted at a battery service station using the original manufacturer's data.

Included in the initialization routine will be an initialization of FullChargeCapacity "full\_cap", RelativeStateOfCharge "SOC" and the RemainingCapacity "Itf" values, as well as state and other variables to ensure a proper start of the capacity calculation. Then, the program resets all system timers such as the calculation of voltage, temperature and selfdischarge

timers before passing out of the initialization routine.  
1 The capacity calculation will then initiated at each trigger signal 17 which is delivered every 500 msec by the external 32 kHz crystal 36.

As explained above, the default values are  
5 necessary to ensure that upon a power-on/ reset, the rechargeable battery capacity calculation (explained below) may be executed. The preferable nominal default values for the critical parameters used for the capacity calculation algorithm 151 and explained in detail in co-  
10 pending patent application (USSN 08/318,004), are set forth as follows:

The DesignCapacity (theoretical or nominal capacity, hereinafter "nom\_cap") may range between 1700  
15 mAh to 2400 mAh, but, after a memory loss, the capacity calculation algorithm defaults to a preferred value of 2000 mAh and the new capacity is relearned from that level; the default value of the number of battery cells  
20 in the rechargeable battery pack is 6 cells, however, this value may be changed depending upon the actual configuration of the battery pack; The AL\_REM\_CAP value represents the remaining capacity alarm triggering value  
25 and may range from 50 mAh to 500 mAh. Preferably, AL\_REM\_CAP has a default value (AL\_REM\_CAP\_DEF) of 200 mAh. An alarm condition exists when the remaining capacity is below this value (without taking into  
30 account the remaining capacity after EDV due to current and temperature (i.e., the residual capacity correction)). The AL\_REM\_TIME value represents the estimated remaining time at the present discharge rate  
and may range from 1.0 min. to 20 min.. Preferably, AL\_REM\_TIME has a default value (AL\_REM\_TIME\_DEF) of 10  
minutes. This alarm condition exists while the calculated remaining time to voltage breakdown (EDV),  
based on the minute average current (discussed below),

-36-

is below the value of AL\_REM\_TIME and will automatically be disabled when the battery is in the charging mode.

1 The AL\_DTEMP value represents the dT/dt alarm trigger condition and may range from 1°K/min. to 5°K/min.. Preferably, AL\_DTEMP has a default value (AL\_DTEMP\_DEF) of 2°K/minute. This alarm condition will exist when the

5 battery detects that the rate of its internal thermal rise (dT/dt) is greater than the AL\_DTEMP value. The AL\_HI\_TEMP value represents the high temperature alarm trigger and may range from 310°K to 345°K. Preferably, AL\_HI\_TEMP has a default value (AL\_HI\_TEMP\_DEF) of

10 328°K. Additionally, when the capacity calculation is started by power-on-reset, the FullChargeCapacity, ("full\_cap" represents the learned full charge capacity of the battery), will be initialized to the

15 DesignCapacity (nom\_cap); the RemainingCapacity ("Itf") to 1/8 of the full\_cap; and, the RelativeStateOfCharge ("soc") to 12.5% and the battery state to capacity decreasing, and, specifically, to selfdischarging mode. The alarm timer N\_ALARM is set at 10 seconds and this is

20 the amount of time that an alarm condition will be broadcast between a host device and/or a battery charger as will be explained in further detail below. It should be understood that these values are typical values for a NiMH battery intended for use in a portable computer. Other types of battery chemistry, or portable devices,

25 may call for a different set of default values.

As shown in Figure 3, after the system is initialized at step 100, the battery will enter into a standby or maintenance mode 23 where it will either

30 awake upon a bus-request signal 15 or awake upon the external crystal trigger signal 17 every 500 msec. If the battery is awaked by a bus request signal 15 as determined at step 21, then the battery will handle the request by the handle request routine indicated at step

35

25 where it will thereafter exit into the standby mode.

1 The routine for handling the requests 25 will be explained in further detail below.

5 If the system is triggered by the normal external crystal trigger signal 17, and there are no bus requests, then the program disables the bus requests (approximately 37 msec before the trigger signal) and enables the A/D converter to begin the current, voltage, and temperature measurements for the current operating cycle as shown at step 130 in Figure 3. A "getvalues" status flag is then checked at step 139 to determine whether A/D conversions of the raw current, voltage, and temperature measurement values are to be performed. When this flag is set high (logic level =1), the raw current, voltage, and temperature values of the rechargeable battery are obtained for the current trigger cycle as shown at step 140. These raw A/D current, voltage and temperature values are built into a special function register 61, as shown in Figure 2(b), which is one of sixteen such registers provided in the hybrid IC for subsequent storage in RAM as I, U, or T. 10 15 20 If the "getvalues" flag is low (logic level =0), then no raw current, voltage, and temperature measurements will be obtained for the present cycle, and the getvalues flag will toggle high (logic 1) at step 148 and the process will continue as shown in Figure 3.

25 After new current, voltage, and temperature values are obtained (step 140), the A/D measurements ready flag is set high (logic level =1) at step 141, and a check is made at step 142 to determine whether the system is in a sample mode. Thus, at step 142, if the absolute value of the raw current,  $|I|$ , is determined to be below a threshold value of 10 mA, then the battery system will operate at half the sample rate depending upon the status of the sample mode flag. Thus, at step 30 35

143 in Figure 3, a determination is made as to whether the sample mode flag is low (i.e., logic 0) or high (logic 1). If the sample mode flag is low, then the sample mode flag will toggle to a high level at step 144, and the system is placed in a sample mode and the process proceeds at step 149 to initiate the A/D conversion. If the sample mode flag is already high (from the previous cycle), then the "getvalues" flag is set equal to zero at step 146, and the A/D converter is disabled at step 147. The A/D conversion will not occur (to save power) and the algorithm proceeds to the capacity calculation (step 151). The "getvalues" flag is always set low in the sample mode. The status of this flag ensures that an A/D conversion will be skipped, and, as a consequence, no new valid data will be available for the capacity calculation at step 150.

If the raw current,  $|I|$ , is determined at step 142 to be above the 10 mA threshold, then the battery system will exit the sample mode (and the sample mode flag is set at logic 0) at step 145, and the A/D conversion of the raw current, voltage, and temperature values will be performed at step 149. At step 150, a determination is made as to whether the A/D measurement ready flag is high (logic 1) indicating that valid raw battery parameter data has been received. If it is set high, then the capacity calculation and attendant battery characteristic conversions (voltage, current, and temperature) will be performed. If the A/D measurement ready flag is low (logic 0), then the capacity calculation is not performed in the current cycle, and the process proceeds to step 158 where the bus request line for message transfer is enabled and the hybrid IC is placed in the sleep mode at step 23. The oscillator trigger 17 continues to wake up the microprocessor every 500 msec, however, when the current



is less than 10 mA, the A/D conversions and the capacity calculations may be performed at an arbitrarily determined rate that is less frequent, for e.g., once every two or once every five seconds, to conserve power.

Figure 8(a) illustrates the timing of the operating cycles under normal mode operating conditions 57a as compared when the system operates under sample mode conditions 57b explained below. As shown in Figure 8(a) and, as mentioned above, the 32 kHz external crystal delivers the trigger signal 17 every 500 msec to initiate the raw voltage, current, and temperature measurements, indicated as 158. Also initiated is the capacity calculation 160 which utilizes the current, voltage, and temperature measurements of the previous operating cycle. When the raw current value obtained is determined to be below a threshold value of 10 mA, the battery system will operate at half power, and no measurements will be taken during the next 500 msec operating cycle as indicated as 58b in Figure 8(a). However, measurements are taken one second later at the next operating cycle as indicated as 58c. When the raw current value obtained is determined to be above a threshold value of 10 mA, the battery system will resume normal mode operation and during the next and subsequent operating cycles, the capacity calculation and attendant battery characteristic measurements (voltage, current, and temperature) will be taken.

Figure 8(b) illustrates the approximate time durations for the various measurements. As a matter of design choice, the capacity calculation 160 is performed in approximately 71 msec for each operating cycle. Thereafter, the alarm control subroutine 152 will be performed for a duration of approximately 29 msec and the charger control subroutine 154 will be performed for a duration of approximately 2 msec if the smart battery

determines these operations are to be performed (see Figure 3). The LED display routine 156 may be performed if it is requested by a user and the LED display control functions will take place for approximately 23 msec as shown in Figure 8(b). It should be understood that the aforementioned performance times for the various routines may vary due to the accuracy of the internal 455 kHz oscillator, which may vary with temperature. Each of the alarm control subroutine 152, charger control subroutine 154 and LED display subroutine 156 will be explained in further detail below.

Since the system management bus request line is inactive during the capacity calculation, alarm control, charger control, and LED display routines, the microprocessor will be unable to receive requests from a host device or battery charger as indicated for the time duration 158 for each operating cycle shown in Figure 8(a). Therefore, in each operating cycle, after the capacity calculation has been performed, the System management bus request line is enabled for the remaining time of the 500 ms cycle, as indicated in Figure 8(b), so that it may respond to a request from a host device or charger. Concurrently, the battery places itself in the standby mode 23 whereupon it will be awaked for the next cycle upon receipt of the system trigger signal 17, or, be awakened by a bus request signal 15 as shown in Figure 3. For a remaining 37 msec of each operating cycle, the bus request is again disabled as shown for the time duration 158 prior to the next trigger signal 17. As mentioned above, each system trigger signal 17 initiates the start of the internal clock 48 generating the 455 kHz signal for controlling the hybrid IC, microprocessor, A/D converter, etc.

Algorithm for calculating battery capacity

1           The purpose of the capacity calculation is to  
continuously monitor the capacity of the rechargeable  
battery in accordance to the formula indicated by  
5   equation (1) as follows:

$$\text{CAP}_{\text{rem}} := \text{CAP}_{\text{rem}} + \sum \epsilon_c I_c \Delta t_c - \sum I_d \Delta t_d - \sum I_s \Delta t_s \quad (1)$$

where  $\text{CAP}_{\text{rem}}$ , is referred to hereinbelow as "Itf" and  
indicates the remaining capacity in the battery at any  
10   given time expressed as mAh (milliampererehours); the  
 $\sum \epsilon_c I_c \Delta t_c$  term represents the sum of the incremental  
increases in capacity as the battery is being charged  
and takes into account a charge efficiency factor  $\epsilon_c$   
accessed preferably from look-up table values to be  
15   explained in further detail below with respect to Figure  
22(c), or, alternatively, may be obtained from a  
response equation or by interpolating between several  
points stored in memory; a  $\sum I_d \Delta t_d$  term which represents  
the sum of the continuous decrease in battery capacity  
20   due to discharge associated with the battery's usage;  
and a  $\sum I_s \Delta t_s$  term which represents the predicted and  
measurable amount of self-discharge based upon self-  
discharging effects associated with the battery's  
chemistry and is a function of the battery state of  
25   charge and temperature. By knowing the  
RemainingCapacity, Itf, at all times, it is possible to  
provide battery parameter information useable by a host  
computer (PC) or smart battery charger to ensure safe  
and reliable battery use and to ensure prolonged battery  
30   life.

Figures 13(a) through 13(b) illustrate the  
capacity calculation routine performed for the  
rechargeable battery pack at each trigger cycle. In

parallel, the current, voltage and temperature  
1 measurements are running except when in the "sample"  
mode where these measurements are taken once every  
second. The sample mode is designed to save power  
consumption (i.e., the A/D conversions occur at half-  
5 frequency) and is switched on and off depending upon the  
amount of detected current. For example, when the  
current falls below 10 mA, the "sample" mode is enabled  
and less frequent measurements are made.

Normally the temperature, voltage and current  
10 are measured and updated once per cycle. The current is  
measured with an integrating method (explained in detail  
below), which recognizes its changes during the  
conversion time. All output values taken from SMBus  
requests and capacity calculation are one period  
15 delayed. The A/D measurements are controlled by an on-  
chip oscillator at nominal 455 kHz and the operating  
cycles - responsible for the integration time - by the  
precise 32 kHz oscillator. The lower accuracy of the  
absolute frequency value of the on-chip oscillator has  
no influence on the accuracy of the measurement.  
20

As shown in Figure 13(a), step 200, the first  
step of the capacity calculation, the IUT Calculation  
routine 200 is performed to first convert the raw  
analog/digital converter output data from register 61  
(Figure 2(b)) into values having appropriate units  
25 useful for the capacity calculation algorithm. Details  
of the IUT Calculation routine can be found in the  
above-mentioned, co-pending patent application (USSN  
08/318,004). Briefly, as illustrated in Figure 12, at  
step 205, the raw A/D Current measurement,  $I_{\text{raw}}$ , is  
30 scaled and converted to the actual current value "I" in  
units of milliamps. Similarly, the raw A/D pack voltage  
measurement,  $U_{\text{raw}}$ , is scaled and converted to the  
actual battery pack voltage value "U" in units of  
35

millivolts. Next, as indicated at step 212, the  $\mu P$  checks the battery pack voltage "U" to determine whether or not the individual cells of the battery pack have an output voltage less than 0.9 V. If a cell is detected as outputting a voltage less than 0.9 volts, then the battery pack is placed in a Sleep mode, as indicated at step 212'. As shown in Figure 12, the following actions take place when the battery state changes between an ON and SLEEP mode:

To save battery power and minimize current drain, the  $\mu P$  proceeds to switch off: the A/D converter 60 at step 213 and 455 kHz on-chip oscillator at step 216. While in the sleep mode, the RAM memory contents are kept alive by voltage from the battery with only memory leakage current drain (which is dependent upon the amount of RAM). Additionally, the wake-up comparator circuit 80 (Figure 11) is activated at step 217 and then the  $\mu P$  sets a bit flag to tell the hardware to start a special voltage control logic to set itself for sleep, as indicated at step 218.

As shown at step 219 in Figure 12, and, as illustrated in Figure 11 the wake-up comparator circuit 80 is periodically activated by a trigger signal 77a derived from the external 32 KHz oscillator. At each period, the comparator is turned on to compare the ratio of pack voltage signal 82 with the predetermined bandgap reference voltage signal 83 that is supplied from the bandgap reference circuit 62 (Figure 4) and input to the inverting input of comparator 76. For a three cell battery pack, the bandgap reference voltage 83 is approximately 1.239 volts, but, this value may be changed in accordance with the battery pack design. When the ratio of pack voltage signal 82  $V_{DD}$  of the ASIC has increased above reference voltage signal 83, then the comparator circuit will toggle, as shown at step

220, to awake the  $\mu$ P and enable the A/D converter again  
1 to take measurements, as indicated at step 221. The  
capacity calculation will then continue with an  
initialization at step 100.

A detailed schematic of the wake-up comparator  
5 circuit 80 is shown in Figure 11. As shown in Figure  
11, the wake-up comparator circuit 80 comprises a  
voltage divider comprising resistors R4 and R5 which are  
tied to the  $V_{DD}$  ASIC power supply to supply a ratio of  $V_{DD}$   
pack voltage (signal 82) to a first non-inverting input  
10 of a comparator 76. As will be explained in further  
detail below, an NMOS (n-channel MOSFET) transistor  
switch 89b connected between resistor R5 and ground is  
nominally turned off in sleep mode to prevent battery  
current drain to ground, but, is periodically turned on  
once every 500 milliseconds (30 microseconds) by trigger  
15 signal 77a to enable the divided  $V_{DD}$  voltage to appear at  
the non-inverting input of the comparator 76.  
Simultaneously, the external oscillator trigger signal  
77a, triggers the wake-up comparator circuit 80 by  
20 simultaneously turning on the transistors 89a,b to  
enable comparator 76 operation. As shown in Figure 11,  
a low power current source 90 which is derived from the  
battery by external circuitry, turns on transistor  
switch 89a, to provide a reference current to comparator  
76. From this current source 90, the working point of  
25 the comparator is fixed. Additionally, enable line 15a  
is tied to signal 77a to simultaneously enable the  
comparator to take a measurement. Transistor switch 89b  
is turned on by signal 77b, which is output from  
inverter 72, to create a path to ground to enable  $V_{DD}$   
30 voltage divider signal 82 to appear at the comparator  
input so that the comparison may be made.

When the  $V_{DD}$  ratio is low ( $< 0.9$  V/cell) and  
the ratio of pack voltage signal 82 is less than the A/D

converter bandgap reference signal 83, then the  
1 comparator output signal 13 is low. When  $V_{DD}$  rises above  
the reference voltage 83, i.e., 3.33 Volts (1.11 volts  
per cell for a three-cell battery pack) the wake-up  
(comparator output) signal 13 goes high, thus, allowing  
5 normal sample mode operation to resume. As shown in  
Figure 11, element 78 is a Schmitt trigger device which  
is a bistable device that is provided at the output of  
the comparator 76 to prevent spurious oscillations  
appearing at the output of the comparator 76 that might  
10 be due to comparator switching characteristics and/or  
amplifier noise.

Due to the low power consumption of the MOS  
circuitry implemented in the hybrid IC, the total  
current consumption of all operating components while in  
the sleep mode is no greater than approximately 2.0  $\mu$ amp  
15 (microamps).

Referring back to Figure 12, as long as each  
cell is detected as outputting a voltage greater than  
0.9 volts, the capacity calculation continues, and, at  
20 step 215, the raw A/D pack current temperature  
measurement,  $T_{raw}$ , is converted to the actual battery  
pack temperature in units of degrees Kelvin. This  
temperature value is additionally scaled to take into  
account thermistor scaling values, (not shown), and a  
final current temperature value of "T" is obtained. At  
25 step 222, the condition of the battery is checked to  
determine if an over temperature condition exists, where  
a temperature of 328°K or greater is detected. When  
detected, a temperature alarm condition flag,  
HI\_TEMP\_ALARM, is set. If capacity is increasing and  
30 the over temperature condition exists then a  
TERMINATE\_CHARGE\_ALARM flag will be set indicating that  
one or more of the battery's charging parameters are out  
of range.

At this point, it should be mentioned that an  
1 end of charge condition may exist (if the capacity is  
increasing). This end of charge condition may be  
detected when the rate change in voltage or temperature  
taken between successive measurements is at a certain  
5 gradient. Thus, as shown in Figure 12 at step 224, and  
described in detail (steps 240 through 249 of Figure  
5(b)) in co-pending patent application (USSN  
08/318,004), the change in temperature  $dT/dt$  calculation  
is performed. Additionally, as shown in Figure 12, a  
10 change in voltage  $dU/dt$  calculation is performed at step  
227.

The change in temperature ( $dT/dt$ ) calculation  
is performed to evaluate the difference  $dT$  between the  
current temperature value  $T$  and a previous temperature  
value determined at a time 20 seconds previously, but  
15 may range anywhere from 10 to 120 seconds previous.  
After the  $dT$  calculation is performed, a determination  
is made as to whether the amount of internal temperature  
change exceeds the allowable rate, i.e., whether the  
AL\_DTEMP alarm condition exists, as shown at step 226 in  
20 Figure 12. A temperature change of approximately  
 $2^{\circ}\text{K}/\text{min}$  or greater indicates an AL\_DTEMP alarm condition  
and, when detected, an alarm condition flag,  
DTEMP\_ALARM, is set.

25 The change in voltage ( $dU/dt$ ) calculation is  
performed to evaluate the difference  $dU$  between the  
current voltage value  $U$  and a previous voltage value  
determined at a time preferably 255 seconds previous.

After the  $dU$  calculation is performed, a  
determination is made at step 260 as to whether the  
30 capacity is decreasing, and, as to whether the present  
voltage  $U$  is less than the end of discharge voltage  
(EDV) limit (typically  $0.9 \text{ V}/\text{cell}$ ), indicating that an  
end of discharge condition EOD\_U exists. Thus, the



present voltage value  $U$  is compared to the preset end of  
1 discharge voltage ( $U_{empty}$ ) to determine if it is less  
than this voltage. If an End of Discharge condition for  
voltage exists, then an  $EOD\_U$  flag is set at step 262  
and a  $Terminate\_Discharge\_Alarm$  flag is set indicating  
5 that the battery has supplied all the its charge, and is  
now nominally fully discharged. If an End of Discharge  
condition does not exist, then the  $EOD\_U$  flag and the  
 $Terminate\_Discharge\_Alarm$  flag are cleared at step 264.  
Additionally, at step 264, the capacity reset flag is  
10 disabled. The IUT\_Calculation procedure 200 is then  
exited and the capacity calculation continues at step  
165 in Figure 13(a).

At step 165 of the capacity calculation  
routine 151 of Figure 13(a), a calculation of the  
15 rolling minute average current is performed utilizing  
the recent previous current ( $I$ ) measurements. Rolling  
minute average current calculations are important for  
calculating battery conditions such as "average time to  
empty" which is based on the average current drain, and  
20 which might be requested by a host device, as will be  
explained in greater detail below. Then, at step 170 of  
Figure 13(a), a determination is made as to whether the  
present current ( $I$ ) value is less than or equal to the  
selfdischarge current  $I\_SELFD$ , which, in the preferred  
25 embodiment, is 3.0 milliamps but may range anywhere from  
2.0 ma to 10.0 ma and represents the limit for a mode  
and battery state recognition. If the present current  
( $I$ ) value is less than or equal to the selfdischarge  
current then the state of the battery is determined to  
30 be capacity decreasing without any external drain.  
Consequently, a selfdischarge flag bit is set at step  
175. If the present current ( $I$ ) value is greater than  
the selfdischarge current (3.0 mA), then the battery  
selfdischarge flag bit is cleared at step 172. The

1 battery self-discharge current is always calculated  
regardless as to whether the battery is in a capacity  
increasing or capacity decreasing state. The direction  
of current is established at step 178 in Figure 13(a) to  
determine the present state of the battery. If the  
5 current (I) is determined to be a positive value, then  
the state of the battery is capacity increasing  
(hereinafter CI) and a capacity increasing flag is set  
at step 180. If the current is determined to be a  
negative value, then the state of the battery is  
10 capacity decreasing (hereinafter CD) and a capacity  
decreasing flag is set at step 182. If it is  
determined that the capacity is decreasing, then a  
determination is made at step 184 as to whether the end  
of discharge voltage (plus hysteresis) EOD\_UH flag has  
been set.

15 For accurate battery parameter presentation  
and battery life predictions, it is important that the  
full battery capacity be reset after an end of discharge  
voltage condition (battery nominally fully discharged)  
has been detected. Even at a nominally discharged  
20 condition, some residual battery capacity remains and  
this is taken into account into the battery calculation,  
as will be explained below. Thus, a determination is  
made at step 189 as to whether the capacity reset flag  
has been set as a result of the EOD\_UH flag having been  
25 set indicating that the battery pack end of discharge  
voltage has been reached (as determined at step 184),  
or, as a result of the battery self discharge flag  
having been set (as determined at step 175), or, if  
capacity is increasing. If the capacity reset flag has  
30 been set, then, at step 190, the remaining capacity  
(Itf) at the EOD voltage condition is reset to a  
predicted Residual Capacity "pd" value obtained from  
look up table depicted in Figure 22(a). Additionally,

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at step 190, the error register is reset to zero and the capacity reset flag is cleared. The program then  
1 proceeds to the selfdischarge calculation and current integration procedures. If, at step 184, the EOD\_UH flag has been determined not to have been set, or, if the  
5 capacity reset flag had not been set as determined at step 189, then the algorithm proceeds at step 192 in Figure 13(b).

As described in further detail (with reference to Figure 6(b) of co-pending patent application (USSN 08/318,004), and in view of step 192 of Figure 13(b), a  
10 state change determination is made for determining whether the state of the battery has changed, i.e., whether the battery has changed from a capacity increasing (CI) state to a capacity decreasing (CD)  
15 state, or vice versa. This step is necessary to avoid the instance of false battery cycle counting or the inaccurate learning of the full charge capacity due to current pulse sign changes or breaks of the current flow.

As indicated from steps 300 to 325 of Figure 13(b), the selfdischarge calculation procedure is  
20 performed. Specifically, as described in further detail (with reference to Figure 6(b) of co-pending patent application (USSN 08/318,004), a 128 second timer for the selfdischarge calculation is first decremented.  
25 Preferably, steps 305-325 of the selfdischarge calculation are performed once every 128 seconds. If the self-discharge timer has not timed out, the program proceeds to step 400 (indicated by broken lines) to perform the current integration procedure 400, as shown  
30 in detail in Figure 13(b) and explained in further detail below.

Selfdischarge calculation routine

1           Due to the electrochemical nature of batteries  
the selfdischarging correction of the remaining capacity  
has to be calculated all the time, independent from the  
5       existence of any charging or discharging currents. This  
is because there will always be a self-discharge current  
drain regardless of whether the battery is being charged  
or discharged and the amount current drain is a function  
of the battery charge and temperature. Thus, as  
10       indicated as step 305 in Figure 13(b), the selfdischarge  
rate "s" as a function of the relative state of charge  
"soc" and current temperature T is accessed via a look-  
up table, shown in Figure 22(b) which shows a three-  
dimensional graphic representation of self-discharge  
15       current (vertical axis) as a function of relative  
battery state of charge and temperature. These look up  
factors "s" for selfdischarge give the predicted  
selfdischarge rate scaled by the design (nominal)  
capacity, and, as is shown in Figure 22(b), the amount  
20       of selfdischarge current,  $I_s$ , generally increases with  
increasing temperature and increased battery state of  
charge levels. For instance, at approximately 65°C and  
a 95% relative state of charge, battery selfdischarge  
current might total an amount of up to 30% of the full  
25       battery capacity per day. The selfdischarge values  
depicted in Figure 22(b) were empirically derived and  
will vary, depending upon the battery chemistry and  
battery architecture.

At step 310, a determination is made as to  
whether the state of the battery is capacity increasing  
30       or capacity decreasing. If the battery is in a  
discharging state, as shown at step 315, the total  
amount of capacity decrease (current drained) since the  
last state change is calculated and stored in a separate

-51-

register. If the capacity is increasing, then the program is directed to step 320, where the effects of the selfdischarge rate is taken into account for the error calculation. Step 320 is also performed after the total amount of capacity decrease (current drained) since the last state change is calculated at step 315. Then, at step 325, the actual capacity integral "Itf" is decremented by the selfdischarge rate "s", thus, providing the  $\Sigma I_{\Delta t}$  in equation (1) described above. Afterwards, the self-discharge procedure ends and the current integration routine 400 is performed.

#### Battery charge integration routine

When the battery is being charged, it is said to be in the Capacity Increasing state (CI), else it is in the Capacity Decreasing state (CD). CD includes the standby mode of the battery, when no current flows through the battery terminals. In the standby mode, only the selfdischarging rate reduces the capacity.

The battery current will be precisely integrated during both charge and discharging states. The capacity integration itself is independent from the battery state, but, as will be hereinafter explained, look up tables (LUT) provide adjustment factors to enable more precise capacity adjustment. For instance, a first LUT (described below with respect to Figure 22(c)) comprises current efficiency factors dependent upon the battery relative state of charge, the C\_rate (current), and the temperature; a second LUT comprising selfdischarging rates dependent upon relative state of charge and temperature; and, a third LUT with residual capacity corrections dependent upon the discharging current rate and temperature which give the fraction of the full capacity which can be extracted from the battery under

-52-

relaxed conditions after the battery has reached an end of discharge voltage condition at a given current rate.

The flow diagram for the current integration process 400 is shown in Figure 13(c). As shown in Figure 13(c) the first step of the current integration process is to determine the magnitude of the relative state of charge (soc). The soc is defined as the actual capacity expressed as a percentage of the full charge capacity (i.e., the capacity of the battery when fully charged) and is used to estimate the amount of charge remaining in the battery. Thus, as indicated at step 405, a determination is made as to whether the remaining capacity is greater than zero (0). If the remaining capacity  $Itf$  is a negative number, the full capacity is incorrect and must be learned and the soc value is clamped to zero (as indicated at step 412 in Figure 13(c)). Otherwise, the soc calculation will take place at step 410. As previously described, until the full charge capacity of the battery is learned, the full charge capacity is initialized as the design (nominal) capacity.

Next, as indicated at step 415 in Figure 13(c), the  $C\_rate$  is calculated. The  $C\_rate$  is defined as the rate in which it would take the energy source to drain in one hour and is measured in units of reciprocal hours. The  $C\_rate$  calculation in step 415 is based on the actual current value ( $I$ ) and the present full charge capacity value and is additionally scaled. A determination is then made at step 418 as to whether the battery is in a capacity increasing or capacity decreasing (discharging) state. If the capacity is increasing, then the battery is being charged and the charge calculation must take into account a charge efficiency factor, made available in a LUT for charge efficiency, accessible by the microprocessor, as

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graphically represented in Figure 22(c). Thus, at step 420 the charge efficiency factor dependent upon the charge current, relative state of charge (soc), and the temperature, is accessed. For instance, as shown in Figure 22(c), when the battery is charged to approximately 95% of full capacity, and the current is being charged at a 0.1 C\_rate at a temperature of 45 °C, the charge efficiency factor  $\epsilon_c$  is found to be about 0.8. The charge efficiency factors are empirically derived and will vary depending upon the battery chemistry and battery architecture. The representations shown in Figure 22(c) are for a battery state of charge 95% and it is understood that charge efficiency values will vary considerably depending upon (remaining capacity) state of charge.

Finally, the increase in charge for the current time interval taking into account the actual current and the charge efficiency factor is calculated at step 435 to form the term  $\epsilon_c I_c \Delta t_c$  in equation (1). This value will be used to increment the integration at step 445 as will be explained below.

If at step 418 it is determined that the capacity is decreasing, the amount of discharge will be integrated for the current discharge cycle as indicated at step 422 in Figure 13(c). It is next determined at step 425 whether the self-discharge flag had been previously set (see step 175, Figure 13(a)) indicating that the battery discharge current is less than 3 mA, and that only the self-discharging processes need to be considered. If the self-discharge flag bit has not been set, a charge calculation is made at step 440 to increment the integration. The final integration is accomplished at step 445 wherein the charge increment calculated at either step 435 or 440 is added to the remaining capacity  $Itf$ , and, as indicated in equation

(1). Additionally, at step 445, the charge is integrated for an error calculation and the running total of the error is also calculated as will hereinafter be discussed in detail.

If it is determined at step 425 that the self-discharge flag has been set (step 175), then the battery is selfdischarging without any external correct drain (step 175, Figure 13(a)) and the residual capacity is calculated at steps 451 through 456. The first step of this routine is to determine the residual battery capacity value. This value, which is dependent upon the current C\_rate and the temperature, is accessed at step 451 by the microprocessor from the look-up table depicted in Figure 22(a). For instance, as shown in Figure 22(a), at a temperature of -20° C and a current drain of twice the C\_rate, (2C), it has been empirically derived that approximately 92% of the full battery capacity will remain when the end of discharge voltage is reached. When applying a light load (e.g., C/10 discharge rate) at a temperature of about 23° C, virtually no residual capacity will remain when end of discharge voltage is reached.

At step 455, a determination is made as to whether the C\_rate is greater than a high discharge threshold rate (preferably of \_\_\_ mAh) and whether the End of Discharge flag (see step 262, Figure 12) had been set. If not, then the capacity calculation at steps 440 and 445 is performed as described above. If the current discharge rate is higher than the high discharge threshold rate, then all of the capacity resets are disabled, as indicated at step 456, and the integration procedure continues at step 440.

During the operational state of the battery, whether the battery capacity is increasing (CI) or decreasing (CD), the end of charge conditions (EOC) and



end of discharge (EOD) conditions, respectively, have to be observed. Therefor, the capacity calculation routine illustrated in Figures 13(a) and 13(b) continues by making a determination as to whether the battery is in a capacity increasing or capacity decreasing (resting or discharging) state, as indicated at step 198 in Figure 13(b). If the capacity is increasing, then the routine for determining whether an End\_Condition CI has been met as indicated at step 500. If the capacity is decreasing, then the routine for determining whether an End\_Condition CD has been met as indicated at step 600.

Observation routine for capacity increasing end conditions

The microprocessor of the hybrid IC calculates a charge termination by one of three methods: a negative voltage slope greater than 10 mV/cell/min  $\pm$  5mV/cell/min at a full charge voltage; a  $\Delta T/\Delta t$  that exceeds 0.9°/min  $\pm$  0.2°/min, or a preferred calculated charge of 120% of full charge capacity (but may range from 100% to 150 % of CAP<sub>FC</sub>). The routine for determining if one of the EOC trigger conditions has been met is illustrated in the flow diagrams of Figures 14(a)-14(d).

If it is determined that the capacity is increasing, then the first step 505 of the EOC (CI state) observation process 500 illustrated in Figure 14(a), is a determination of whether the battery's relative state of charge (soc) value is greater than 20% of the battery's full charge capacity value. If the battery has attained that level of capacity, then the fully discharged status flag is cleared at step 507. As will be explained below, the fully discharged status flag is set when it is determined that the battery has

-56-

supplied all the charge it can without being damaged. Until the battery reaches that capacity level, the FULLY\_DISCHARGED status flag will remain set. Next, as indicated at step 510, the first EOC trigger detection method is performed. This first method is a determination as to whether the  $dT/dt$  trigger enable condition has been met, and, whether the slope of the temperature increase  $dT$  is greater than or equal to a threshold limit indicating an EOC condition. In the preferred embodiment, the  $dT/dt$  trigger enable condition is satisfied whenever the relative state of charge (soc) is above a 50% threshold limit, and, an end of charge condition is detected when the slope of the temperature increase becomes greater than a threshold of about  $0.9^{\circ}\text{C}/\text{min}$ . It should be mentioned that the slope of the temperature may trigger EOC when it is detected within the range from  $0.5^{\circ}\text{C}/\text{min}$  to  $12^{\circ}\text{C}/\text{min}$ . If either of these conditions are not satisfied, then a second method of detecting an EOC condition, namely, a detection of whether the slope of the voltage change,  $dU/dt$ , becomes negative wherein the value of  $dU/dt$  must have a minimum amount and the charging current rate ( $C_{\text{rate}}$ ) must be greater than a certain value, is performed at step 540 as will be explained in further detail below. If the  $dT/dt$  trigger enable condition has been met and the slope of the temperature increase  $dT$  is greater than or equal to the EOC threshold limit, then a determination as to whether the EOC flag has been set is made at step 512. When the EOC flag has not been set, then the number of cells in the battery pack will have to be learned - a process indicated as element 700 in Figure 14(b) to be described below. Whether or not the number of cells in the battery pack is learned (as will be explained below), at step 700, then step 570 is performed wherein: a) the EOC status flag is set; b) the

35

remaining capacity is set equal to 95% of the full  
charge capacity; c) the error registers are cleared; d)  
1 the overflow flag for the uncertainty calculation is  
cleared; and, e) the fully charged status flag is set  
indicating that the battery has reached a charge  
5 termination point. Finally, the algorithm proceeds to  
step 575, shown in Figure 14(c), where the terminate  
charge alarm flag is set.

If the  $dT/dt$  trigger enable condition has been  
met, the slope of the temperature increase  $dT$  is greater  
than or equal to the EOC threshold limit, and the EOC  
10 flag has been set (step 512), then a determination is  
made at step 514 as to whether the remaining capacity  
( $Itf$ ) is greater than or equal to the full charge  
capacity. If this condition is satisfied, then the  
remaining capacity is set to the full charge capacity as  
15 indicated at step 520. Additionally, at step 520, the  
error registers are cleared and the overflow flag for  
the uncertainty calculation is cleared. If the  
remaining capacity ( $Itf$ ) is not greater than or equal to  
the full charge capacity (step 514) then the algorithm  
20 proceeds to step 575, shown in Figure 14(c), where the  
terminate charge alarm flag is set. In the preferred  
embodiment, the terminate charge alarm flag must be set  
when the battery detects EOC on any of the EOC trigger  
conditions or when an over temperature condition exists,  
25 i.e., if  $T \geq AL\_HI\_TEMP$  (step 222, Figure 12)). As  
explained above, the terminate charge alarm flag may  
already be set by the 95% full-trigger, which is  
initiated when the first temperature slope trigger  
condition is satisfied at step 510.

30 After the remaining capacity is set to the  
full charge capacity at step 520, the algorithm proceeds  
at step 530 to determine whether the battery charger is  
still on. This is accomplished by checking for a

positive charge increase obtained during the charge integration process (see step 435, Figure 13(c)). If the charger is still on, then it is known that the charger is continuing to overcharge the battery, and the algorithm must keep track of the amount of battery overcharge. Thus, at step 532 in Figure 14(a), the total amount of overcharge is calculated by adding the charge increase to the overcharge registers (not shown). It should be mentioned that the overcharge register is never reset, so that the total amount of overcharging since the system start-up is retained. Whether or not the battery charger is still on, the algorithm proceeds to step 535 where the overcharging alarm status flag is set indicating that the battery is being charged beyond an EOC indication. Finally, the algorithm proceeds to step 575, shown in Figure 14(c), where the terminate charge alarm flag is set.

As mentioned above with respect to step 510, if either the  $dT/dt$  trigger enable condition has not been met, or, the slope of the temperature increase  $dT$  is not greater than or equal to the EOC threshold limit, then a second method of detecting an EOC condition is performed at step 540 shown in Figure 14(c). At step 540, a determination is made as to whether: a) the charge is constant current, i.e., whether the difference between the current value and the average current value for one (1) minute is preferably less than 50 milliamps; b) whether the  $dU/dt$  voltage change is negative and is greater than a threshold amount of preferably 12 mV/m; and, c) whether the charge current is greater than a predetermined rate, preferably, a rate of  $C/10$ . If either of the second method EOC trigger conditions are not satisfied, then a third method of detecting an EOC condition, namely, a detection of whether the relative state of charge (soc) is above 120% and the current rate

is between C/50 and C/5 is performed at step 545. It should be mentioned that the EOC condition may be triggered when the relative state of charge (soc) is detected within the range of 100% to 160%. If all of the second method EOC trigger conditions are satisfied, or, if all of the third method EOC trigger conditions are satisfied, then a determination as to whether the EOC flag has been set, is made at step 550 in Figure 14(c). If either the second method EOC trigger conditions or third method EOC trigger conditions are satisfied, and the EOC flag has been set (step 550), then the fully charged status flag is set at step 555 indicating that the battery has reached a charge termination point. Afterwards, the process proceeds at step 520, Figure 14(a), by clamping the remaining capacity value to the full charge capacity value as described above. If the EOC flag has not been set, then the number of cells might have to be learned- a process indicated as element 700 to be described below. When the process of learning the amount of cells in the battery is complete, then the EOC status flag will be set at step 551, and the fully charged status flag is set at step 555 indicating that the battery has reached a charge termination point and the algorithm continues at step 520 described above. If all three EOC trigger conditions are not satisfied, then the EOC detection procedure 500 is exited and the capacity calculation (Figure 6(b)) continues.

Alternately, a -dU trigger condition will be reached when it is determined that the battery capacity is increasing,  $dU > DU\_MIN$ , where  $DU\_MIN$  is a predetermined value equal to the number of battery pack cells multiplied by 10mV, and the current is determined to be constant and the charge rate is higher than 0.3C. The charge current is considered constant if  $|I - I\_avg|$

-60-

1  $|I - I^{-1}| < 50 \text{ mA}$  and  $|I - I^{-1}| < 50 \text{ mA}$  where  $I^{-1}$  was the  
previous value of the current measurement. The  
constancy of the battery charging may be calculated in  
addition to, or, in place steps 250 et seq. of the IUT  
calculation routine Figure 5(b), where the method of  
calculating  $-dU$  may be accomplished without time  
5 dependency.

#### Learn number of cells routine

As described above, an emergency power-down  
condition may occur wherein all RAM contents are lost.  
10 In such a situation, it may be necessary to relearn the  
number of cells in the battery pack. Rather than  
burning in the number of cells for a particular battery  
module in the ASIC ROM, the number of cells may be  
learned to enable the ASIC to be configured with other  
15 battery packs having a different number of cells. The  
relearning of the number of cells is indicated by a bit  
(CALIBRATED bit) in the AL\_STATUS register, which will  
indicate whether the number of battery cells has to be  
relearned. In the preferred embodiment, it is easily  
20 accomplished by utilizing the voltage measured at the  
battery pack terminals after an EOC condition, described  
above, is met.

The first step 705 in the learn number of  
cells procedure 700 shown in Figure 14(d), is to  
25 determine whether the battery pack is uncalibrated,  
i.e., whether the CALIBRATED bit in the AL\_STATUS  
register indicates that the number of cells should be  
learned. If so, it is determined at step 710 whether  
the converted voltage value,  $U$  (mV), measured at step  
30 210, Figure 5(a) during the IUT calculation procedure,  
is greater than 11 volts. If so, then it is concluded  
that the battery pack has nine (9) cells and the number  
of cells is set at nine in step 720. If the measured

35

-61-

1 voltage value,  $U$ , is not greater than 11 volts, then a  
determination is made at step 715 as to whether the  
voltage is greater than 7.5 volts. If so, then it is  
concluded that the battery pack has six (6) cells and  
the number of cells is set at six in step 725. If the  
5 measured voltage value,  $U$ , is not greater than 7.5  
volts, then it is concluded that the battery pack has  
four (4) cells and the number of cells is set at four in  
step 730. After the number of cells is determined, the  
EOD cutoff voltage,  $U_{empty}$ , is set equal to the number  
of cells multiplied by the operating battery voltage of  
10 1.02 volts in the preferred embodiment as indicated at  
step 740 in Figure 14(d).

15 Observation routine for capacity decreasing end  
conditions

As previously mentioned, the capacity  
calculation routine 151 at step 198 makes a  
determination as to whether the battery is in a capacity  
increasing or capacity decreasing (resting or  
20 discharging) state. If it is determined that the  
capacity is decreasing, then the first step 605 of the  
EOD (CD state) observation process 600 illustrated in  
Figures 15(a) and 15(b), is a determination of whether  
the present voltage measurement ( $U$ ) is greater than the  
25 end of discharge voltage (EDV) and any hysteresis. When  
the EDV voltage is reached, it is an indication that  
discharging should be stopped to save the battery from  
damage. Typically, the EDV is 1.02 V/cell. If the  
voltage obtained is greater than the EDV voltage, then a  
30 flag indicating that the voltage is greater than the EDV  
voltage plus hysteresis is set at step 610. If the  
voltage is not greater than the EDV voltage plus  
hysteresis, then the flag is cleared at step 612.

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-62-

1 Additionally, as indicated at step 613, since the capacity is decreasing, the Terminate Charge Alarm and Over Charging Alarm flags are cleared.

5 A determination as to the value of the remaining capacity (Itf) is made at step 615, where it is determined whether the remaining capacity is less than the calculated error (i.e., the uncertainty capacity). If the remaining capacity is less than the calculated error, then this is an indication that the battery pack has no more capacity and is fully discharged. Consequently, the FULLY\_DISCHARGED status flag is set at step 618 and the process continues at step 619. If there is remaining capacity, then the FULLY\_DISCHARGED flag is not set, and the process continues at step 619 where a determination of the relative state of charge is made. If the relative state of charge (soc) has dropped below some hysteresis value, preferably, about 80% of the full charge capacity, then the FULLY\_CHARGED status flag is cleared, as indicated at step 620. Whether the FULLY\_CHARGED status flag is cleared or not, the process continues at steps 625 and 630, where the cycle count number is updated. At step 625, a determination is made as to whether a cycle count flag is cleared, and, whether the capacity has decreased by 15% of nominal capacity. If these two events of step 625 have occurred, then the cycle count register, containing a value of the number of times the battery has been charged or discharged (not shown), will be incremented at step 630 and the cycle count flag will be set. It should be understood that in the preferred embodiment, the cycle count will be incremented whether or not the battery has been fully or partially charged. Whether the cycle count flag is incremented or not, the process continues at step 640, where a check is made as to whether the EOD flag is set, and, whether the reset

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-63-

flag is clear. If either the EOD flag is not set, or, the reset flag is not clear, then the end condition observation routine 600 is exited. If the EOD flag is set, and, the reset flag is clear, then a determination is made at step 645 as to whether the EOC (end of charge) flag has been set and whether the error value (uncertainty capacity) is less than 8% of nominal capacity. If these conditions are satisfied then the full charge capacity value is learned at step 650. Specifically, whenever the battery has performed a full cycle reaching an EOC trigger point and the EOD point and the uncertainty capacity is below 8% of the nominal capacity, the full charge capacity is reset at step 650 with the formula:

$$\text{full\_cap} = \text{full\_cap} + \text{full\_cap} \cdot \text{pd}/256 - \text{Itf}$$

where "pd" is the predicted residual capacity correction value accessed from the look-up table of Figure 22(a) and dependent upon the discharging current rate and temperature. The divisor 256 provides for an integer scaling of pd. The meaning of the formula is to exchange the remaining capacity (Itf) by the residual capacity from the LUT table, which contains fractions of the full charge capacity (Note: the residual capacity obtained is calculated from step 451 of the charge integration process of Figure 13(c)). If the EOD point is reached with less capacity output as in the former cycle, the amount of Itf (remaining capacity) will be higher at EDV (less discharged capacity compared with the accumulated charged capacity). The full charge capacity will be reduced by the difference of Itf compared with the former cycle so that the ageing of the battery is taken into account by this learning step. If the battery is used in several partial charge/discharge

cycles without reaching an EOC or EOD point, the error  
of the calculation can accumulate to a heavy difference  
1 between the real capacity and the calculated remaining  
capacity (Itf). The algorithm (MaxError()), to be  
explained in detail below, calculates the maximum  
5 possible error (uncertainty) during its operation as  
precise as the capacity integration itself on the base  
of a percentile error for each operating mode. The  
uncertainty is reset to zero at each EOC and EOD point.  
An uncertainty of above 8% disables the full capacity  
reset. Additionally, when the conditions at step 650  
10 are satisfied, the EOC flag is cleared indicating that  
the full charge capacity has been reset. After the full  
charge capacity is reset (step 650), or, if it is  
determined that the uncertainty error is greater than  
the prespecified value of 8%, or, the EOC flag is not  
15 set, then the algorithm continues at step 655.

At step 655, a determination is made as to  
whether the C\_rate at the EDV (end of discharge voltage)  
trigger is equal to zero, or, whether the present C\_rate  
is less than the C\_rate at the EDV trigger, and, whether  
20 the capacity reset is not disabled. If either of these  
conditions are satisfied, the present current at the EOD  
trigger is set equal to the present C\_rate, the delayed  
capacity reset value is set equal to the present  
residual capacity value, and, the flags to delay  
25 capacity reset after EOD are set at step 660. Else, if  
both of the conditions of step 655 are not met, then the  
end conditions observation routine 600 is exited.  
As indicated in Figure 13(b) of the capacity calculation  
routine 151, if the EOC and EOD triggering has not  
30 occurred, then the capacity calculation is exited.

System management bus and bus interface

1 As described above, and as shown in Figures  
2(a) and 2(b), a modified Phillips I<sup>2</sup>C bus interface is  
used by the battery module 28 to communicate within a  
5 configuration comprising the ASIC 32 and the battery 10,  
a host computer 16, and a smart charger 22. As  
mentioned previously, requests are either from the host  
computer to the battery, from the charger to the  
battery, or, from the battery to either the host or  
10 charger. An example of a typical communication between  
the battery and the charger may be to switch the charger  
on and off, or, to demand a certain charging rate. The  
host computer may request information of the battery  
such as the battery state, or, the battery alarm  
15 conditions such as minimal capacity, or,  
overtemperature. The bus interface control circuit 75  
controls all requests and alarm conditions via two  
serial ports SMBCLK and SMBDATA over the system  
management bus.

20 When the battery 10 needs to inform the host  
of an alarm condition or to inform the battery charger  
about its desired charging voltage or current, the  
battery acts as a bus master with write function  
capabilities. The battery will function to: evaluate the  
request from the  $\mu$ P 50; check if the system management  
25 bus is free;  
generates a start bit and sends the address of the  
battery charger or host; checks whether the ACK-bit has  
been sent from the charger or host and gives a message  
to the  $\mu$ P; sends the data supplied from the  $\mu$ P on the  
30 bus and checks for ACK bit; generates a stop-bit at the  
end of the transfer.

When the battery 10 is requested by the host  
to provide it with information to be explained below,

-66-

the battery acts as a bus slave with read and write capabilities. For instance, during the steady-state operation, the host might request some information from the battery and will formulate a request. Figure 16 illustrates the software algorithm compatible with the system management bus interface protocol for providing communication between an external device (host PC or battery charger), and the battery, which acts as a slave thereto.

Specifically, the first step 750 in Figure 16, is to decode the command code that has been sent by the external device. Illustrative command codes are discussed hereinbelow, and each typically requires two bytes of data to be transmitted which is indicated as the variable "count". The next step, indicated as step 752, is to determine whether the command code sent is a valid, recognizable command word. If not, a unsupported command bit is set at step 755 and the transmission will be terminated as indicated at step 758a in Figure 16. If the command is supported, the battery will perform an internal check to determine if an error has occurred at step 759. If an internal error is found, then the algorithm will enter a timer loop which will keep checking the internal flag until an error is confirmed or the timer (not shown) times out. This is indicated at step 761. If a correct value is found at step 759, then the algorithm will continue at step 764 to determine if the decoded command code calls for a read or write function. If the timer has timed out, or, an error is confirmed at step 761, then an unknown error flag is set at step 763 and the software transmission is terminated at step 758b.

When functioning as a slave, the battery will perform either read or write functions. At step 764, a determination is made as to whether the command code

input (step 750) is a read or write command. If it is a  
1 read command, a determination is made at step 765 as to  
whether the battery is to perform a calculation as  
requested by the external device and return a value to  
be read by the external device. Examples of  
5 calculations made by the battery in response to a query  
(for e.g., AvgTimeToEmpty()) from a host device are  
described in greater detail below. The battery  $\mu$ P will  
proceed to perform the calculations at step 768 and will  
return a data value to a specified address location as  
10 indicated by the read block routine at step 800 and  
explained in detail below. If it is determined at step  
765 that a calculation is not to be performed, (for  
e.g., only a voltage value is requested) then the  
algorithm will proceed directly to the read block  
15 routine 800 as shown in Figure 16.

If, at step 764, it is determined that a write  
function is to be performed wherein a data value is to  
be written to the battery address location from an  
external device, (for e.g., the AL\_REM\_TIME threshold  
20 value), then a write block authorization check must be  
performed to determine if the external device may  
perform the write function. This is indicated at step  
771 where a password is checked for validity. If the  
password checked is not an authorized password, then  
25 access will be denied as indicated at step 774, and the  
external device will not be able to perform the write  
function and will terminate the software transmission at  
step 758b. If the external device is authorized to  
write data to a battery address, then the device will  
30 write a data value to pre-specified address locations,  
as indicated by the write block routine at step 775 to  
be explained in detail below.

Host to Smart Battery Communication

1       A host to smart battery communication  
transfers data from the battery to either a user (of a  
host PC, for e.g.), or, the power management system of  
an external device. A user can get either factual data,  
5       such as battery characteristic data, (Voltage(),  
Temperature(), charge/discharge Current(),  
AverageCurrent() etc.), or, predictive (calculated) data  
such as the battery's remaining life at the present rate  
of drain, or, how long it will take to charge the  
battery. It should be mentioned that a real load,  
10       e.g., a host PC monitor, has a constant power  
consumption. When remaining time values described below  
are calculated (using the assumption that the currents  
are constant), errors and inaccuracies may occur. Thus,  
15       it should be considered to assume a constant power  
consumption of the load when calculating the remaining  
time and other variables. Thus, in the following  
calculations such as RemainingCapacityAlarm(), AtRate(),  
RemainingCapacity(), FullChargeCapacity(), and  
20       DesignCapacity() ..., average power values may be  
utilized as an alternative to average current values.

The following control commands are  
representative of battery supplied information when  
queried by a host device or host PC:

25       The RemainingCapacity() function returns the  
battery's remaining capacity and is a numeric indication  
of remaining charge. Depending upon the capacity mode  
bit, the RemainingCapacity() function will return a  
value in mAh or 10mWh. The value returned is calculated  
as follows:

30       Itf[mAh] - Itf\_err[mAh]

where the uncertainty error `Itf_err` is the subtracted value and the output value is cut at 0 if (`|Itf| < |Itf_err|`).

The `RemainingCapacityAlarm()` function sets or retrieves the low capacity threshold value `AL_REM_CAP` (described above) for the low capacity alarm value stored in RAM. When the `RemainingCapacity()` falls below the `AL_REM_CAP` value, the battery sends Alarm Warning() messages to the host with the `REMAINING_CAPACITY_ALARM` bit set. At manufacture, the `AL_REM_CAP` value is set to 10% of design capacity and will remain unchanged until altered by the `RemainingCapacityAlarm()` function. This function is used by any host system that desires to know how much power it will require to save its operating state. It enables the host system to more finely control the point at which the host will transfer to a low power mode.

The `RemainingTimeAlarm()` function sets or retrieves the `AL_REM_TIME` alarm value. When the estimated remaining time at the present discharge rate as calculated by the `AverageTimeToEmpty()` function falls below the `AL_REM_TIME` value, the battery sends Alarm Warning() messages to the host with the `REMAINING_TIME_ALARM` bit set. An `AL_REM_TIME` value of zero (0) effectively disables this alarm and the value is initialized to 10 minutes at time of manufacture. The `FullChargeCapacity()` function returns the predicted or learned battery pack capacity when it is fully charged and is expressed either in current (mAh or 10mWh) depending upon the setting of the `CAPACITY_MODE` bit (discussed below). The `DesignCapacity()` returns the theoretical capacity of a new battery pack which when compared with the value returned by the `FullChargeCapacity()`, will provide an indication of the

-70-

battery wear. This information is useful by a host device or host PC to adjust its power management policy.

The AtRate() function is the first half of a two-function call-set used to set the AtRate value used in calculations based on capacity made by the AtRateTimeToFull(), AtRateTimeToEmpty(), and, AtRateOK() functions.

When the AtRate value is positive, the AtRateTimeToFull() function returns the predicted time, preferably in minutes, to fully charge the battery at the AtRate value of charge (value is in mA or 10 mW). The calculation formula is governed by equation ( ):

$$\text{time} := 60 * \frac{(\text{full cap[mAh]} - \text{Itf[mAh]})}{|\text{AT\_RATE}|}$$

( )

where "time" is the returned value in minutes.

The AverageTimeToFull() function returns the predicted remaining time in minutes until the battery is full if a current like the last minute rolling average, I\_avg, value is continued. The calculation formula is governed by equation ( ):

$$\text{time} := 60 * \frac{(\text{full cap[mAh]} - \text{Itf[mAh]})}{\text{I\_avg}}$$

( )

where "time" is the returned value in minutes.

When the AtRate value is negative, the AtRateTimeToEmpty() function returns the predicted operating time, preferably in minutes, at the AtRate value of battery discharge, until the battery will be exhausted (EDV condition). The calculation formula is governed by equation ( ):



-71-

$$\text{time} := 60 * \frac{(\text{Itf}[\text{mAh}] - \text{full\_cap}[\text{mAh}] * \text{pd\_at\_rate}/256 - \text{Itf\_err}[\text{mAh}])}{|\text{AT\_RATE}|}$$

1

where "time" is the returned value in minutes,  $|\text{AT\_RATE}|$  and  $\text{pd\_at\_rate}$  values are calculated by the  $\text{AtRate}()$  function where  $\text{pd\_at\_rate}$  represents the remaining capacity (fraction of full\_capacity) and is divided by the value of 256 to scale that value to a fraction.  $\text{Itf\_err}$  is the uncertainty error as explained below.

When the  $\text{AtRate}$  value is negative, the  $\text{AtRateOK}()$  function returns a Boolean value that predicts the battery's ability to supply the  $\text{AtRate}$  value of additional discharge energy for 10 seconds, i.e., if the battery can safely supply enough energy for an additional load after the host PC sets the  $\text{AtRate}$  value.

The  $\text{RunTimeToEmpty}()$  function returns the predicted remaining battery life at the present rate of discharge (minutes) and is calculated based on either current or power depending upon the setting of the  $\text{CAPACITY\_MODE}$  bit (discussed below). The value returned by this function can be used by the host PC or device power management system to get information about the relative gain or loss in remaining battery life in response to a change in power policy. The calculation formula is governed by equation ( ):

25

$$\text{time} := 60 * \frac{(\text{Itf}[\text{mAh}] - \text{full\_cap}[\text{mAh}] * \text{pd}/256 - \text{Itf\_err}[\text{mAh}])}{|I|[\text{mA}]}$$

where "time" is the returned value in minutes and takes into account the remaining capacity in the battery after EDV which can be get out only by reduction of the load;  $|I|$  is the current,  $\text{pd} := \text{pd}(\text{C\_rate}(|I|, T)$  and is calculated in the capacity calculation algorithm  $\text{pd}$

35

-72-

represents the remaining capacity (fraction of full\_capacity). This value is divided by 256 to obtain a fraction. Itf\_err is the uncertainty error as explained below.

The AverageTimeToEmpty() function returns a one-minute rolling average of the predicted remaining battery life (in minutes) and is calculated based on either current or power. This function provides an averaging of the instantaneous estimations, thereby ensuring a more stable display of state-of-charge information. The calculation formula is governed by equation (\_):

$$\text{time} := 60 * \frac{(\text{Itf}[\text{mAh}] - \text{full\_cap}[\text{mAh}] * \text{pd\_avg}/256 - \text{Itf\_err}[\text{mAh}])}{\text{I\_avg}[\text{mA}]}$$

where "time" is the returned value in minutes, I\_avg is updated every 0.5 sec, pd\_avg := pd(C\_rate(I\_avg), T) and is calculated in the alarm\_control routine one cycle before and represents the predicted residual capacity (fraction of full\_capacity). This value is divided by 256 to obtain a scale fraction. Itf\_err is the uncertainty error as explained below.

Figure 23 illustrates two voltage versus time graphs, a and b, comparing calculated battery capacity characteristics at various discharging current rates for a six (6) cell battery pack. As shown in Figure 23, graph a, the voltage will rapidly decrease to an end of discharge condition in a short amount of time when a load amounting to a discharge rate of 2C and yielding approximately 1.554 Ah (amperehours) is applied to the battery. When the load is significantly decreased to a C/5 discharge rate, the battery pack voltage will generously rise to extend the life of the battery for an amount of time to yield another 0.816 Ah. Graph b,

which is of a different time scale than graph a, shows  
 1 that discharge at the C\_rate will yield approximately  
 2.307 Ah. When that load is lightened to one half the  
 C\_rate, the battery voltage will increase slightly and  
 the battery life can be predicted to extend for an  
 5 amount of time to yield another .078 Ah until end of  
 discharge voltage is reached.

As discussed above, certain calculations are  
 dependent upon the value of the uncertainty capacity,  
 i.e., the maximum possible error obtained during the  
 capacity calculations. The MaxError() function returns  
 10 the actual uncertainty in the capacity calculation in  
 percentage. A MaxError() output of 20% means that the  
 real value may be between 10% below and 10% above the  
 internally calculated capacity. Most of the  
 15 calculations in the system management bus interface  
 already subtracts the uncertainty error, so that the  
 error will be -0/ + MaxError()%. The uncertainty is set  
 to zero on EOC and EOD conditions by the capacity  
 algorithm as explained above. The calculations  
 performed are as follows:

$$\text{Itf\_err} := \text{Itf\_err\_C\_D} * \text{EPS}/256 + \frac{\text{Itf\_err\_S} * \text{EPS}}{256}$$

$$\text{max\_error} := 2 * 100 * \text{Itf\_err}[\text{mAh}]/\text{full\_cap}[\text{mAh}]$$

25 where Itf\_err\_C\_D is the always positive accumulated  
 charge during the charging and discharging mode;  
 Itf\_err\_S is the accumulated charge of the  
 self\_discharging process. Because of the permanent  
 30 presence of selfdischarging, even while charging, this  
 accumulation is done all the time using the LUT  
 dependency from relative state of charge (soc) and  
 temperature. Both accumulators are reset to zero at EOC  
 and EOD condition. EPS is the error fraction of the

capacity calculation -especially from the LUT and from  
1 A/D measurement - while charging or discharging, with  
the scaling factor 256 applied. EPS\_S is the error for  
selfdischarge-charge integration as fraction. The  
uncertainty will grow undesirable if the battery will  
5 not be fully or discharged over several cycles and the  
learn mode of the full capacity will be disabled.

The CycleCount() function returns the number  
of charge/discharge cycles the battery has experienced.  
The cycles count on each charge decrease with the amount  
10 of 15% of the design capacity after the last recharging,  
which needs not to be a full charging.

Other registers contained in the DBOS memory  
scheme is the BatteryMode() register which is used to  
select the battery's various operational modes. For  
instance, the BatteryMode() register is defined as  
15 containing a CAPACITY\_MODE bit which is set to specify  
whether capacity information is to be broadcast in units  
of mAh or mWh (milliwatthours). This bit allows power  
management systems to best match their electrical  
characteristics with those reported by the battery. For  
20 example, a switching power supply is best represented by  
a constant power model, whereas a linear supply is  
better represented by a constant current model.  
Additionally, the BatteryMode() register contains a  
CHARGER\_MODE bit which is set to specify whether  
25 charging voltage and charging current values are to be  
broadcast to the smart battery charger 22 (Figure 1)  
when the smart battery requires charging. This bit  
allows a host PC or battery charger to override the  
smart battery's desired charging parameters by disabling  
30 the smart battery's broadcast of the charging current  
and charging voltage.

Another function calculated on the basis of  
capacity is the BatteryStatus() function which is used

by the power management system of a host device or PC to  
1 get alarm and status bits, as well as error codes from  
the battery status register. This function returns the  
battery's status word flags including alarm warning bits  
such as OVER\_CHARGED\_ALARM, TERMINATE\_CHARGE\_ALARM,  
5 DTEMP\_ALARM, OVER\_TEMP\_ALARM, TERMINATE\_DISCHARGE\_ALARM,  
REMAINING\_CAPACITY\_ALARM, and, REMAINING\_TIME\_ALARM and  
status bits including INITIALIZED, DISCHARGING,  
FULLY\_CHARGED, and, FULLY\_DISCHARGED.

Ancillary functions that the battery 10 is  
capable of performing include: the SpecificationInfo()  
for providing the version number of the smart battery  
specification the battery pack supports; the  
ManufactureDate() for providing a system with  
information that can be used to uniquely identify a  
15 particular battery; the Serial Number(), which provides  
information for identifying a particular battery; the  
ManufacturerName() function returns the name of the  
smart battery's manufacturer; the DeviceName() function  
returns a character string that contains the battery's  
name; the DeviceChemistry() returns a character string  
20 that contains the battery's chemistry; the  
ManufacturerData() function which allows access to the  
manufacturer data (e.g., lot codes, number of deep  
cycles, discharge patterns, deepest discharge, etc.,  
25 contained in the battery.

#### Write Block Routine

As mentioned above, the battery may receive  
30 data from an external device to be used in a control  
command calculation, or, as an alarm threshold value.  
The write block 775 illustrated in Figure 17, controls  
this transfer of data to the battery. First, at step  
776, a determination is made as to whether the data

-76-

value to be read from the external host device is  
1 greater than two bytes long. In the preferred  
embodiment, most control commands will write a data  
value to the battery that is two bytes long. If the  
data is longer than two bytes, i.e., if count > 2, then  
5 the variable "w" is set equal to the number of address  
locations allocated for and corresponding to length of  
data in number of bytes at step 778. Then, at step 780,  
a determination is made as to whether the previously  
determined count value has been set equal to the address  
10 locations allocated. If this is not the case, then an  
error flag is set at step 790 indicating that an  
inordinate amount of data is to be sent, or, that there  
is not enough locations allocated for receiving the  
data. If the previously determined count value "count"  
15 has been set equal to the number of address locations  
allocated, then the program enters a loop indicated as  
steps 781, 783 and 785 wherein each byte of data is  
sequentially written to the I<sup>2</sup>C bus to the battery  
address location [Adr] (step 783). After each byte is  
20 sent, the count of the number of bytes is decremented  
and the address location for the next sequential data  
byte to be written is incremented. Until count = 0,  
indicating that the last byte of data has been  
transmitted to the battery as shown at step 785, the  
25 loop will continue and enter at step 781 to determine if  
the battery has read each data byte (RDVAL = 1) sent by  
the external device and indicating that the data byte  
has been successfully transmitted. If the read  
acknowledge flag has been received after each byte  
30 transfer, the loop continues at step 783 until the last  
data byte is sent. If the read acknowledge flag has not  
been received, then an error may have occurred and the  
program proceeds to step 782 where a determination is  
made as to whether a bus error or timeout has occurred.

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-77-

If none of these instances has occurred, then the program will proceed to step 787 to determine if the bus master has terminated the transmission. If the bus master has terminated the transmission, then an error flag is set at step 790 indicating that an inordinate amount of data is being transmitted and the transmission will be terminated at step 795. If the bus master has not terminated the transmission, then the system will continue to look for the RDVAL flag until an internal handshake timer (not shown) times out (step 782) and an unknown error flag is set and the transmission will be terminated, as shown at steps 792 and 795. In view of Figure 17, it is understood that in some cases, a fixed two-byte data word is to be read, as indicated at step 776, and the algorithm will proceed directly to step 783 where the first data byte is read by the battery at the first battery address location.

After the last data byte has been received, as indicated at step 786, a determination is made as to whether the stop bit flag has been received from the modified I<sup>2</sup>C bus master indicating the end of bus control due to the fact that the external device will not be sending any more data. If the stop bit is received the write block routine is exited. If the stop bit has not been received, then an error may have occurred and the program proceeds to step 788 where a determination is made as to whether a bus error or timeout has occurred. If an error or timeout has occurred, then the program will proceed to set an unknown error flag and the transmission will be terminated, as shown at steps 792 and 795. If none of these instances has occurred, then the program will proceed to step 789 to determine if the RDVAL flag has been set to indicate if the last data byte has been successfully read. If it has been successfully read, then this is an indication that the

-78-

external device has not finished sending data or that not enough address locations have been allocated and an error flag will be set as shown at step 790 and the transmission will be terminated at step 795. If the last data value has been successfully read at step 789, then the process will continue to look for the modified I<sup>2</sup>C bus master stop bit at step 786 until either an internal handshake timer (not shown) times out or an error occurs (step 788).

#### 10 Read Block Routine

As mentioned above, the battery will return a calculated or measurement data value to a specified address location as indicated by the read block routine 800 as illustrated in Figure 18. At step 802, a determination is first made as to whether the data value to be written to the host device is greater than two bytes long. If the data is longer than two bytes, i.e., if count > 2, then the address is pointed to at step 805 and the program enters a loop indicated as steps 808, 812, and 815 wherein each byte of data is sequentially written to the SMBus bus to an address location of the requesting host device as indicated at step 812. After each byte is sent, the count of the number of bytes is decremented and the address location for the next byte to be written is incremented. Until count = 0, indicating that the last byte of data has been transmitted to the external device as shown at step 815, the loop will continue and enter at step 808 to determine if the acknowledge bit has been sent by the external device indicating that the current data byte has been successfully transmitted. If the acknowledge bit has been received after each byte transfer, the loop continues at step 812 until the last data byte is sent.

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1 If the acknowledge bit has not been received, then an  
error may have occurred and the program proceeds to step  
2 821 where a determination is made as to whether a bus  
error, termination, or timeout has occurred. If none of  
these instances has occurred, then the program will  
5 proceed to step 808 to again determine if the data byte  
acknowledge bit has been received. This process will  
continue until an internal handshake timer (not shown)  
times out wherein the process will continue at step 825  
where an unknown error flag is set and the transmission  
10 will be terminated. After it is determined that the  
last data byte has been sent (step 818) then a flag  
indicating that the last byte has been sent is set at  
step 818 of Figure 18. In view of Figure 18, it is  
understood that in some cases, no data is to be returned  
15 as shown at step 802, and the algorithm will proceed  
directly to step 812 and bypass the receipt  
acknowledgment bit step 808.

Next, as indicated at step 822, a  
determination is made as to whether the stop bit flag  
20 has been received from the I<sup>2</sup>C bus master indicating the  
end of bus control due to the fact that the external  
device will not be receiving any more data. If the stop  
bit is received the read block is exited. If the stop  
bit has not been received, then an error may have  
25 occurred and the program proceeds to step 824 where a  
determination is made as to whether a bus error or  
timeout has occurred. If none of these instances has  
occurred, then the program will proceed to step 822 to  
again determine if the stop bit has been received. This  
30 process will continue until an internal handshake timer  
(not shown) times out wherein the process will continue  
at step 825 where an unknown error flag is set and the  
transmission will be terminated.

Alarm Control

1 All of the alarm status flags heretofore  
mentioned indicate that the battery has reached a  
certain state of charge (fully charged, empty  
5 discharged) or a critical state (maximal temperature,  
being overcharged). These events are encoded in the  
Al\_Status battery register and the warning message  
AlarmWarning() is sent by the battery to an  
external device when the battery detects an alarm  
condition. In this event, the battery becomes the bus  
10 master and alternately notifies the host computer or  
battery charger of any critical and/or alarm conditions  
at a rate of preferably once every five seconds, until  
the critical state is corrected. The alarm condition  
15 may be broadcast to the host computer for 10 seconds if  
the alarm condition is such that the battery charger  
does not need to be notified of an alarm condition, for  
e.g., the REMAINING\_CAP\_ALARM warning message is not the  
broadcast to the charger device. If alarm conditions  
20 such as OVER\_CHARGED\_ALARM, TERMINATE\_CHARGE\_ALARM,  
DTEMP\_ALARM, OVER\_TEMP\_ALARM, and  
TERMINATE\_DISCHARGE\_ALARM exist, then the alarm is  
broadcast, alternating between the charger device and  
the host device, in five (5) second intervals.

25 The modified SMBus protocol for communicating  
alarm or warning messages are illustrated in the alarm  
control routine 152 as shown in detail in Figure 19.  
This routine runs through all possible alarm conditions  
for possible broadcast to a host device after a capacity  
calculation is performed as shown in Figure 3.

30 The first step, indicated as step 901 in Figure 19  
is to verify the status of the remaining capacity.  
Specifically, a determination is made as to whether the  
AL\_REM\_CAP run value is greater than 0 and that the

remaining capacity (less the uncertainty error) is less  
than the AL\_REM\_CAP value. If these conditions hold  
1 true, the REMAINING\_CAPACITY\_ALARM bit is set at step  
904. If none of these conditions holds true, the  
REMAINING\_CAPACITY\_ALARM bit is cleared at step 906.  
5 Next, the C\_rate based on the one minute rolling average  
current is calculated and the residual capacity based on  
the C\_rate [pd\_avg := pd(C\_rate(I\_avg), T)] is accessed  
from the look-up table of Figure 22(a). Then, at step  
910, a determination is made as to whether the battery  
10 state is capacity decreasing. If the battery capacity  
is decreasing, then a determination is made at step 913  
as to whether the AL\_REM\_TIME alarm threshold value is  
greater than zero (0). If so, then the estimated  
remaining time at the present discharge rate is  
15 calculated at step 915 by the AverageTimeToEmpty()  
command code. When the calculated remaining time falls  
below the AL\_REM\_TIME threshold value, as determined at  
step 917, the program sets the REMAINING\_TIME\_ALARM bit  
as indicated at step 919 and the program proceed at step  
20 925 shown in Figure 19. If, it is determined either  
that the battery state is not capacity decreasing (step  
910), or, that the AL\_REM\_TIME is equal to zero (step  
913), or, that the calculated remaining time falls below  
the AL\_REM\_TIME threshold value (step 917), then the  
25 program clears the REMAINING\_TIME\_ALARM bit as indicated  
at step 921 and the program proceed at step 925 shown in  
Figure 19.

As shown at step 925, the upper byte of the  
Alarm status register is checked to determine if any  
alarm bits, e.g., alarm bits such as OVER\_CHARGED\_ALARM,  
30 TERMINATE\_CHARGE\_ALARM, DTEMP\_ALARM, OVER\_TEMP\_ALARM,  
TERMINATE\_DISCHARGE\_ALARM, REMAINING\_CAPACITY\_ALARM,  
and, REMAINING\_TIME\_ALARM have been set. If so, then a  
check of the alarm broadcast flag "alarming" is made at  
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-82-

step 927. If the upper byte of the Alarm status register indicates no alarm condition, i.e., no bits set, then the process will continue at step 926 and the alarming broadcast flag is cleared. Note, that upon initialization, the alarming broadcast flag is not set. However, as long as an alarm condition exists, this flag will be set. Therefore, as shown at step 927, if the alarming flag is cleared, the process continues and the alarming flag is set at step 930. Additionally, at step 930, the alarm broadcast timer is set to zero, and, the "alarm to host" flag is set indicating that the alarm will be sent to a host external device and not a battery charger. The process continues at step 933, where a determination is made as to whether the alarm broadcast timer has timed out (=0). Since the broadcast timer has been set to zero at step 930 for this first operating cycle of the alarm condition, or, if the alarm broadcast timer has timed out, then the process will continue at step 935. If the timer has not timed out, then the alarm control process is exited. At step 935, the address location for the alarm broadcast is set to the host device, and the command code is set equal to the battery status [BatteryStatus()] function described above. This will initiate the transfer of the particular alarm to the host device. A determination is then made at step 937 as to whether the alarm to host flag is cleared (=0). During the first operating cycle of the alarm condition (step 930), the alarm to host flag had been set (=1) so the algorithm skips over steps 940 and 943 (discussed below) and performs the send message routine 945 which changes the function of the battery as having bus master control so that the alarm message can be sent. Details of the send message routine 945 will be explained in detail below. Afterwards, at step 947, the broadcast alarm timer is

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1 reset to its 10 second time (N\_ALARM) and the alarm sent  
to host flag is toggled to the alarm sent to charger  
flag.

5 After the message is initiated to broadcast an  
alarm warning message to the host device at step 945 (by  
the send message routine), and, the alarm broadcast  
timer has been reset, then the process continues. After  
the next capacity calculation (Figure 3), if the alarm  
condition still exists (i.e., the alarm bits are set) at  
step 925, the process is continued. However, for the  
10 next and subsequent operating cycles of the alarm  
condition, the alarming flag has already been set as  
determined (at step 927), so the alarm broadcast timer  
(initialized as 10 seconds) is decremented at step 931  
until the timer has timed out or the alarm status has  
been changed. Thus, after the broadcast timer has  
15 decremented, the process continues at step 933, where a  
determination is made as to whether the alarm broadcast  
timer has timed out (=0). If the broadcast timer has  
not timed out, then the alarm control routine is exited  
and these set of steps will continue until the alarm  
20 broadcast timer has timed out (step 933). Until the  
alarm message has been broadcast to the host device for  
preferably five (5) seconds, then steps 935 and 937 will  
not be performed. When the broadcast timer has timed  
out, and, since the alarm to host flag has toggled  
25 (during the first operating cycle of the alarm  
condition), the condition at step 937 will be true.  
Therefor, the address location for the alarm broadcast  
is changed and set to the battery charger at step 940,  
and the program will proceed to step 943 where a  
30 determination is made as to whether the particular alarm  
warning message is meant to be sent to the battery  
charger for the next 10 seconds. If, the alarm  
condition is not meant to be transmitted to the battery  
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charger, then the send message routine (step 945) will  
1 be bypassed, and the broadcast timer will be reset at  
step 947 and the alarm to host bit toggled so that the  
message will be retransmitted to the host device.

#### 5 Charger Control

Whenever the BatteryMode() CHARGER MODE bit is  
set to zero, and the battery detects the presence of a  
smart battery charger, the battery is able to  
10 communicate with the smart battery charger and will send  
ChargingCurrent() and ChargingVoltage() values to the  
smart battery charger. The ChargingCurrent() function  
sets the maximum current that a smart battery charger  
may deliver to the battery and will return the desired  
15 charging rate in mA. This allows the battery charger to  
dynamically adjust its output current to match optimal  
recharging requirements. A maximum value of 0xFFFF  
means constant voltage charging with the output value of  
ChargingVoltage(). Results are broadcast with the  
20 battery as active bus master under the conditions set  
forth in the charger control routine 154 of Figures 3  
and 20.

The first step 850 in Figure 20 is to  
determine whether the battery is in the system. If not,  
CAPACITY\_MODE and CHARGER\_MODE variables are cleared at  
25 step 853 and the routine is exited. If the battery is  
installed in the system, a determination is made at step  
855 as to whether the battery was just inserted in the  
system. If the battery was just inserted, then the  
message timer is set to one (1), and the CAPACITY\_MODE  
30 and CHARGER\_MODE variables are cleared at step 857 and  
the algorithm continues at step 859. If the battery has  
not just been inserted (step 855), then the algorithm  
skips to step 859 where a determination is made as to

-85-

the state of the charger mode bit. If the bit is not cleared at step 859, then the routine is exited. If the CHARGER\_MODE bit is set at step 859 then the timer is decremented at step 861. The next step at 863 is to determine whether the message timer has timed out. If it has, then the message timer is reset at step 865 and the charging current calculation is additionally made. If the message timer has not timed out at step 863, then the routine is exited. The next step 866 is to determine whether the returned value of the calculated charging current is zero. If the charging current value returned is zero, then the process proceeds at step 868. If the charging current is not zero, then the determination is made at step 867 as to whether the state is capacity increasing (CI). If the battery is in a CI state, then the process proceeds at step 868. If the capacity is decreasing, then the routine is exited.

At step 868, the address location for the charger broadcast is set to the battery charger, and the command code is set equal to the command code ChargingCurrent(). Next, at step 870, the charging current command message is sent to the battery charger by the send message routine (discussed below). Then, at step 872, the maximum value (hex FFFF) fed into the ConstantVoltage() function which indicates that the charger will be a constant current charging device. This instruction is broadcast to the charger via the send message routine at step 874. After the charging current is broadcast, the routine is finally exited.

### 30 Send Message Routine

As indicated at step 945 in Figure 19 and step 870 in Figure 20, the send message routine changes the function of the battery to have bus master control so

that the alarm messages can be sent. Figure 21 illustrates the send message routine.

1       The first step 950 is to determine the data bus  
availability. If it is determined that the data bus is  
available, then the first piece of data to be sent is  
5       the slave address, i.e., the address of the external  
host device or battery charger, as indicated at step  
952. As soon as the data bus is acquired, then two  
flags are set; the first flag is an internally  
generated flag that is set to indicate that the battery  
now has bus master control (step 953), and, the second  
10       flag is the transmission termination flag that is  
cleared at step 954. The next step, as indicated at  
step 955, is a check as to whether the acknowledge bit  
has been sent, i.e., whether the first byte of data  
(slave address) has been received by the slave device.  
15       If the acknowledge bit has not been sent, then a check  
is made at step 958 to determine if the bus is busy. If  
the bus is now busy, then the program continues at step  
960 of Figure 21. If the bus is not busy at step 958,  
then a determination is made as to whether a bus error  
20       or timeout flag has been generated at step 959. If an  
error or timeout has occurred, then the program will  
proceed to step 973 where the transmission will be  
terminated and the routine exited. If an error or  
timeout condition does not exist, the routine will  
25       continue at step 955 until an acknowledge bit has been  
sent by the slave indicating that the data has been  
received. If the acknowledge bit has been received,  
then the current command code is transmitted at step  
957. It should be understood that when the send message  
30       routine is invoked during a critical alarm condition,  
then the command code word is set to the battery address  
(see step 935, Figure 19) and the slave will recognize  
that only two bytes of data are to be sent. The next



-87-

step, as indicated at step 960, is a check as to whether the acknowledge bit has been sent, i.e., whether the command code (or battery address) has been received by the slave device. If the acknowledge bit has not been received, then a check is made at step 962 to determine whether a bus error or timeout flag has been generated. If an error or timeout has occurred, then the program will proceed to step 973 where the transmission will be terminated and the routine exited. If an error or timeout condition does not exist, the routine will continue at step 960 until it is acknowledged that the command code (or battery address) has been received. If the acknowledge bit has been received, then the first byte of data is transmitted to the specified address location (see step 935, Figure 19) at step 965. The next step, as indicated at step 966, is a check as to whether the acknowledge bit has been sent, i.e., whether the first byte of command code data has been received by the slave device. If the acknowledge bit has not been received, then a check is made at step 967 to determine whether a bus error or timeout flag has been generated. If an error or timeout has occurred, then the program will proceed to step 973 where the transmission will be terminated and the routine exited. If an error or timeout condition does not exist, the routine will continue at step 966 until it is acknowledged that the first data byte has been received. If the acknowledge bit has been received, then the second byte of data is transmitted to the next address location at step 968. The next step, as indicated at step 969, is a check as to whether the acknowledge bit has been sent, i.e., whether the second byte of command code data has been received by the slave device. If the acknowledge bit has not been received, then a check is made at step 971 to determine whether a bus error or timeout flag has

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-88-

1 been generated. If an error or timeout has occurred,  
then the program will proceed to step 973 where the  
transmission will be terminated and the routine exited.  
If an error or timeout condition does not exist, the  
routine will continue at step 969 until it is  
5 acknowledged that the second data byte has been  
received. After the full message has been transmitted  
by the battery to the slave device, the send message  
routine is exited.

#### 10 LED display

As shown in Figure 2(a), the battery 10 of the  
instant invention provides manually controlled four (4)  
segment light emitting diode (LED) display indicating  
the relative state of charge of the battery (similar to  
15 a fuel gauge) with respect to the full\_cap value. After  
the capacity calculation, alarm control 152, and charger  
control 154 routines are performed during each 500 msec  
period (operating cycle), the system will look for a  
hardware trigger of the LED display. At any time, a  
user can initiate the LED display by a switch 35 on the  
20 battery 10 as shown in Figure 2(a). The control logic  
for generating the LED display is described in detail  
(in view of steps 975 through 996 of Figure 15) in co-  
pending patent application (USSN 08/318,004).

25 While the invention has been particularly shown  
and described with respect to the preferred embodiments  
thereof, it will be understood by those skilled in the art  
that the foregoing and other changes in form and details  
may be made therein without departing from the spirit and  
scope of the invention, which should be limited only by the  
30 scope of the appended claims.

-89-

## WHAT IS CLAIMED IS:

1. A smart battery having a power management system, and comprising:
  - terminal means for connecting the smart battery to a battery powered device, the terminal means including first and second terminals;
  - a plurality of rechargeable battery cells connected to the terminal means, said battery cells having
    - i) a discharge mode for supplying electrical power to the first and second terminals and to the battery powered device, and
    - ii) a charge mode for receiving electrical power from the terminal means;
  - sensing means for sensing and generating analog signals representing battery voltage, battery temperature, and current at said first and second terminals;
  - an integrated circuit including
    - i) an analog-to-digital converter having abled and disabled states, wherein in the abled state, the converter receives said analog signals and converts said analog signals to digital signals representing battery voltage, battery temperature, and current at said first and second terminals,

-90-

ii) a switching network connected to the sensing means and to the analog-to-digital converter, for receiving the analog signals from the sensing means and transmitting the analog signals, one at a time, to the analog-to-digital converter,

iii) a processor connected to the analog-to-digital converter for receiving the digital signals therefrom, and for performing a predefined series of calculation using said digital signals,

iv) a memory area for storing data values including values representing battery voltage, battery temperature, and current at said first and second terminals,

v) an internal oscillator for generating internal clock signals at a first frequency,

wherein each of said calculations includes a series of timed steps, and the timing of said steps is controlled by the clock signals from the internal oscillator;

an external oscillator for generating clock signals at a second frequency;

means connecting the external oscillator to the processor to transmit to the processor the clock signals from the external oscillator; and

a comparator circuit connected to the sensing means to receive the analog signal representing battery voltage, and to generate a wake-up signal, and to transmit the wake-up signal to the

-91-

processor, when the battery voltage is above a predetermined voltage level;

wherein the processor has (i) a normal mode, (ii) a standby mode, and (iii) a sleep mode,

in the normal mode, the processor performs said series of calculations at first regular cycles each of said first cycles being started by receipt by the processor of one of the clock signals from the external processor,

in the standby mode, the processor performs said series of calculations at second regular cycles, said second cycles being longer than said first cycles, each of said second cycles also being started by receipt by the processor of one of the clock signals from the external processor, and

in the sleep mode, the processor does not perform said series of calculations, and the processor places the analog-to-digital converter in the disabled mode; and

wherein, the processor enters the standby mode when the battery current fall below a preset current level, the processor enters the sleep mode when the battery voltage falls below a preset voltage level, and the processor enters the normal mode when the processor receives the wake-up signal from the comparator circuit.

2. A battery according to Claim 1, wherein the battery cells have a variable capacity, and said

-92-

series of calculations includes calculating a value representing remaining capacity of the battery cells

3. A battery according to Claim 1, wherein:  
the battery has a nominally fully discharged voltage value;

the memory area of the integrated circuit receives operating power from the battery cells and requires a minimum operating voltage to maintain said stored data values; and

said minimum operating voltage is below said nominally fully discharged voltage value, wherein the memory area maintains said stored data values even when the battery is nominally fully discharged.

4. A battery according to Claim 1, wherein:  
the length of each of the second cycles is an integer multiple of the length of each of the first cycles.

5. A battery according to Claim 1, wherein the analog-to-digital converter, the processor, the memory area and the internal oscillator receive operating power from the battery cells.

6. A battery according to Claim 1, wherein:  
the integrated circuit further includes data receiving means to receive data from the battery powered device;

said receiving means has an abled state and a disabled state;

-93-

in the abled state, the receiving means is able to receive data from the battery powered device; and

in the disabled state, the receiving means is disabled from receiving data from the battery powered device.

7. A battery according to Claim 6, wherein: each of the first cycles includes first and second intervals; and

during each of the first intervals of the first cycles, the processor (i) performs said series of calculations, and (ii) places the receiving means in the disabled state to inhibit the transmission of data to the processor from the battery powered device while the processor is performing said calculations.

8. A battery according to Claim 1, wherein the processor performs additional calculations, said additional calculations including calculating a value representing a learned full charge capacity of the battery.

-94-

9. A smart battery having a power management system, and comprising:

first and second terminal means for connecting the smart battery to a battery powered device and to a battery recharger;

a plurality of rechargeable battery cells connected to the first and second terminal means, said battery cells having

i) a discharge mode for supplying electrical power to the first and second terminal means and to the battery powered device, and

ii) a charge mode for receiving electrical power from the first and second terminal means;

sensing means for sensing and generating analog signals representing battery voltage, battery temperature, and current at said first and second terminal means;

an integrated circuit including

i) an analog-to-digital converter for receiving said analog signals and converting said analog signals to digital signals representing battery voltage, battery temperature, and current at said first and second terminal means,

ii) a processor connected to the analog-to-digital converter for receiving the digital signals therefrom, and for performing a predefined series of calculations using said digital signals, and



-95-

iii) a memory area for storing data values including values representing battery voltage, battery temperature and current at said first and second terminal means;

a power supply subcircuit electrically connecting the memory area of the integrated circuit to the battery cells to supply electrical power to said memory area;

a capacitor connected to the battery cells to receive electrical power therefrom, and connected to the memory area to supply electrical power thereto, wherein in case of an interruption of the supply of electrical power to the memory area through the power supply subcircuit receives electrical power from the capacitor; and

a delatching circuit for decoupling the memory area of the integrated circuit from the battery cells, by means of the power supply subcircuit, under predetermined conditions.

10. A battery according to Claim 9, wherein:

the integrated circuit includes a power terminal; and

the power supply subcircuit includes

i) means electrically connecting the battery cells to said power terminal to supply electrical power to said power terminal from the battery cells, and

ii) means electrically connecting the power terminal to the memory area of the integrated circuit

-96-

to supply electrical power to said memory area from the power terminal.

11. A battery according to Claim 10, wherein the delatching circuit electrically decouples the memory area of the integrated circuit from the power terminal when the voltage of the power terminal falls below a given level.

12. A battery according to Claim 11, wherein:

the de-latching circuit includes

i) a switching transistor located in the means electrically connecting the power terminal to the memory area,

ii) a sensor for sensing, and for generating a signal representing, the voltage of the power terminal, and

iii) means for applying to the switching transistor the signal representing the voltage of the power terminal;

the switching transistor has

i) a conductive state for electrically coupling the memory area of the integrated circuit to the power terminal, and

ii) a non-conductive state for electrically decoupling said memory area from the power terminal; and

the switching transistor switches from the conductive state to the non-conductive state when the

-97-

voltage of the power terminal falls below the given level.

13. A battery according to Claim 9, further including means to inhibit the flow of current through the battery cells in case of a short circuit across the first and second terminal means, and to help maintain the flow of current from the battery cells to the memory area of the integrated circuit in case of said short circuit.

14. A battery according to Claim 13, wherein the means to inhibit the flow of current through the battery cells includes a fuse located in series between the battery cells and one of the terminal means.

15. A battery according to Claim 13, wherein the means to inhibit the flow of current through the battery cells includes a positive temperature coefficient element located in series between the battery cells and one of the terminal means, for creating a high impedance between the battery cells and said one of the terminal means in case of said short circuit.

16. A battery according to Claim 13, wherein:

in case of an interruption of the supply of electrical power to the memory area from the battery cells, said memory area receives electrical power from the capacitor for at least a given period of time; and

-98-

in case of a short circuit across the first and second terminal means, the means to inhibit the flow of current through the battery cells raises the voltage of the battery above said preset level within said given period of time.

17. A battery according to Claim 9, wherein:

the battery cells have a variable capacity;  
and

said series of calculations include

- i) calculating a value representing remaining capacity of the battery cells, and
- ii) calculating a value representing learned capacity of the battery cells.

18. A battery according to Claim 9, wherein:  
the battery has a nominally fully discharged voltage value;

the memory area of the processor requires a minimum operating voltage to maintain said stored data values; and

said minimum operating voltage is below said nominally fully discharged voltage value, wherein the memory area maintains said stored data values even when the battery is nominally fully discharged.

-99-

19. A smart battery having a power management system, and comprising:

first and second terminal means for connecting the smart battery to a battery powered device and to a battery recharger;

a plurality of rechargeable battery cells connected to the first and second terminal means, said battery cells having

- i) a discharge mode for supplying electrical power to the first and second terminal means and to the battery powered device, and
- ii) a charge mode for receiving electrical power from the first and second terminal means;

sensing means for sensing and generating analog signals representing battery voltage, battery temperature, and current at said first and second terminal means;

an integrated circuit including

- i) an analog-to-digital converter for receiving said analog signals and converting said analog signals to digital signals representing battery voltage, battery temperature, and current at said first and second terminal means,

- ii) a processor connected to the analog-to-digital converter for receiving the digital signals therefrom, and for performing a predefined series of calculations using said digital signals, and

-100-

iii) a memory area for storing data values including values representing battery voltage, battery temperature and current at said first and second terminal means; and

a data bus for transmitting data between the battery powered device and the integrated circuit;

wherein the integrated circuit further includes (iv) a bus controller to control the transmission of selected data over the data bus; and

wherein the analog-to-digital converter includes

i) a bandgap reference circuit to provide a preset analog voltage, and

ii) a voltage shifting circuit to provide a variable base reference voltage to facilitate generating digital values representing positive and negative analog current signals.

20. A smart battery according to Claim 19, wherein the analog-to-digital converter further includes (iii) a voltage divider network to receive the preset analog voltage from the bandgap preference circuit and to divide said preset analog voltage into a plurality of voltage output values.

21. A smart battery according to Claim 19, wherein the analog-to-digital converter further includes a sigma-delta converter for receiving the analog signals from the sensing means and for converting said analog signals to digital values

-101-

representing battery voltage, battery temperature, and current at said first and second terminal means.

22. A smart battery according to Claim 21, wherein the sigma-delta converter processes each of the analog signals representing battery voltage, battery temperature, and current at said first and second terminal means for a respective period to produce the digital values representing battery voltage, battery temperature, and current at said first and second terminal means.

23. A smart battery according to Claim 22, wherein:

the integrated circuit further includes

v) an oscillator for generating clock signals at a given frequency, and

vi) means to transmit said clock signals to the sigma-delta converter; and

each of said periods has a length determined by said clock signals.

24. A smart battery according to Claim 23, wherein:

the sigma-delta converter processes the analog signals representing battery voltage, battery temperature, and current at said first and second terminal means for first, second and third periods respectively; and

the lengths of said first, second and third periods are determined by the lengths of time required for the sigma-delta converter to receive,

-102-

respectively, first, second and third numbers of the clock signals.

25. A smart battery according to Claim 19, wherein the voltage shifting circuit includes:

a first capacitor having first and second opposite sides;

means to generated a reference ground voltage level; and

a switching network for applying the reference ground voltage level and the analog signals to the first and second sides of the capacitor to develop a voltage level at the capacitor;

the switching network having

i) a first state for applying the reference ground voltage level to the second side of the capacitor, and for applying the at least one of said analog signals to the first side of the capacitor.

26. A smart battery according to Claim 25, wherein:

the analog-to-digital converter further includes a sigma-delta converter including

i) means to generate a second reference voltage level,

ii) an integrator having first and second inputs,

iii) means to apply the second reference voltage level to the first input of the integrator, and



-103-

iv) a switch electrically located in series between the first capacitor and the second input of the integrator; and

the switch has

i) a conductive state for applying the voltage level of the first capacitor to the second input of the integrator, and

ii) a non-conductive state for electrically decoupling the first capacitor from the second input of the integrator.

27. A smart battery according to Claim 26, wherein the sigma-delta converter further includes:

a second capacitor electrically located in parallel with the integrator; and

a further switch electrically located in parallel with the second capacitor to selectively discharge said second capacitor.

28. A smart battery according to Claim 26, wherein:

the integrator has an output voltage level;

the sigma-delta converter further includes

v) a comparator having first and second inputs,

vi) means to apply the second reference voltage level to the first input of the comparator, and

vii) means to apply the output voltage level of the integrator to the second input of the comparator;

-104-

the comparator has

i) a first output when the voltage level applied to the first input of the comparator is less than the voltage level applied to the second input of the comparator, and

ii) a second output when the voltage level applied to the first input of the comparator is greater than the voltage level applied to the second input of the comparator.

29. A smart battery according to Claim 28, wherein:

the sigma-delta converter further includes a counter, and

means for applying the output of the comparator to the counter; and

the counter maintains a count of the number of times the comparator has the first output during a defined period of time.

-105-

30. A smart battery system having a power management system, and comprising:

first and second terminal means for connecting the smart battery to a battery powered device and to a battery recharger;

a battery including a rechargeable battery cell connected to the first and second terminal means, said battery having charge/discharge cycles, each of said cycles having

i) a discharge mode for supplying electrical power to the first and second terminals and to the battery powered device, and

ii) a charge mode for receiving electrical power from the terminal means;

sensing means for sensing and generating analog signals representing battery voltage, battery temperature, and current at said first and second terminal means;

an integrated circuit including

i) an analog-to-digital converter for receiving said analog signals and converting said analog signals to digital signals representing battery voltage, battery temperature, and current at said first and second terminal means,

ii) a processor connected to the analog-to-digital converter for receiving the digital signals therefrom, and for performing predefined calculations using said digital signals, and

-106-

iii) a memory area for storing data values including values representing battery voltage, battery temperature and current at said first and second terminal means; and

a data bus for transmitting data between the battery powered device and the integrated circuit;

wherein the integrated circuit further includes (iv) a bus controller to control the transmission of selected data over the data bus;

wherein said predefined calculations include calculating an actual full capacity of the battery at predefined times.

31. A smart battery system according to Claim 30, wherein:

the processor includes means to identify the ends of at least selected ones of the charge/discharge cycles; and

the processor calculates the actual full capacity of the battery at the ends of at least selected ones of the charge/discharge cycles.

32. A smart battery system according to Claim 31, wherein:

the processor maintains

i) an uncertainty values representing an uncertainty in the full capacity of the battery, and

ii) a nominal full capacity value representing a nominal full capacity of the battery;

after each identified end of one of the charge/discharge cycles, if the uncertainty value is

-107-

less than a given percentage of the nominal full capacity value, then the processor calculates the actual full capacity of the battery.

33. A smart battery system according to Claim 31, wherein:

the processor further includes

i) means to determine a correction value,  
and

ii) means to determine the capacity of the battery at the ends of the charge/discharge cycles;  
and

at the end of a given charge/discharge cycle,

when the processor calculates a new value for the actual full capacity value of the battery, the processor calculates said new value according to the equation

$$nCAP_{FC} = oCAP_{FC} + (oCAP_{FC})x - CAP_{REM}$$

where:

$nCAP_{FC}$  is the new value for the actual full capacity of the battery,

$nCAP_{FC}$  is the most recently previously calculated value for the actual full capacity of the battery,

$x$  is the correction value determined by the processor, and

$CAP_{REM}$  is the capacity of the battery at the end of the given charge/discharge cycle.

34. A smart battery system according to Claim 33, wherein the means to determine the

-108-

correction value includes means to determine the correction value based on battery temperature and battery current.

35. A smart battery system according to Claim 34, wherein:

the means to determine the correction value includes:

a look-up table having a multitude of stored values; and

means to select one of said stored values based on the battery temperature and battery current.

36. A smart battery system according to Claim 32, wherein the predefined calculations further include calculating the uncertainty value at predetermined times.

37. A smart battery system according to Claim 36, wherein the uncertainty value is reset to zero at given times.

38. A smart battery system according to Claim 37, wherein:

each charge/discharge cycle has a charging cycle and a discharging cycle;

the processor includes means to detect a plurality of predefined end of charge conditions during each charging cycle, and to terminate the charging cycle when one of said conditions is detected; and

-109-

the processor resets the uncertainty value to zero when one of said end of charge conditions is detected.

39. A smart battery system according to Claim 37, wherein:

each charge/discharge cycle has a charging cycle and a discharging cycle;

the processor includes means to detect a plurality of predefined end of discharge conditions during each discharging cycle, and to terminate the discharging cycle when one of said conditions is detected; and

the processor resets the uncertainty value to zero when one of said end of discharge conditions is detected.

40. A smart battery system according to Claim 37, wherein:

each of the charge/discharge cycles has a charging cycle and a discharging cycle;

the processor includes means to determine the accumulated amount of current conducted to the battery during the charging cycle of each charge/discharge cycle; and

when the uncertainty value is calculated during one of the charging cycles, the calculated uncertainty values is based on the accumulated amount of current conducted to the battery during said one charging cycle.

-110-

41. a smart battery system according to Claim 37, wherein:

each of the charge/discharge cycles has a charging cycle and a discharging cycle;

the processor includes means to determine the accumulated amount of current discharged from the battery during the discharging cycle of each charge/discharge cycle; and

when the uncertainty value is calculated during one of the discharging cycles, the calculated uncertainty value is based on the accumulated amount of current discharged from the battery during said one charging cycle.



-111-

42. a combination portable computer-rechargeable battery-battery recharger, comprising:

- (a) a portable computer;
- (b) a rechargeable battery system including first and second terminal means connected to the portable computer,

- a rechargeable battery including at least one rechargeable battery cell connected to the first and second terminal means, said battery having
  - i) a discharge mode for supplying electrical power to the first and second terminal means and to the portable computer,

- ii) a charge mode for receiving electrical power from the first and second terminal means
- sensing means for sensing and generating analog signals representing battery voltage, battery temperature, and current at said first and second terminal means;

- an integrated circuit including

- i) an analog-to-digital converter for receiving said analog signals and converting said analog signals to digital signals representing battery voltage, battery temperature, and current at said first and second terminal means,

- ii) a processor connected to the analog-to-digital converter for receiving the digital signals therefrom, and for performing predefined calculations using said digital signals, and

-112-

iii) a memory area for storing data values including values representing battery voltage, battery temperature and current at said first and second terminal means;

(c) a battery re-charger connected to the first and second terminal means for supplying electrical power to said terminal means and to the rechargeable battery cell;

(d) a data bus connected to the portable computer, the battery system and the battery re-charger to transmit data between the portable computer, the battery system and the battery re-charger;

wherein the portable computer includes means for sending and receiving messages over the data bus, said messages including a charge request message to the battery recharger to supply electrical charge to the battery;

wherein the battery re-charger includes means to receive messages transmitted over the data bus, and means to supply electrical charge to the battery in response to receipt by the battery re-charger of said charge request message;

wherein said predefined calculations include one calculation for calculating the remaining capacity of the battery, said one calculation being a function of (i) battery temperature, (ii) the amount of charge supplied by the battery when the battery is in the discharge mode, and (iii) the amount of charge

-113-

received by the battery when the battery is in the charge mode.

43. A combination portable computer-rechargeable battery-battery recharger according to claim 42, wherein:

said one calculation is made at predefined intervals;

at each of said intervals,

i) if the battery is in the discharge mode, the processor determines the amount of charge supplied by the battery since the most recent previous one of said intervals, and the

ii) if the battery is in the charge mode, the processor determines the amount of charge supplied to the battery since the most recent previous one of said intervals.

44. A combination portable computer-rechargeable battery-battery recharger according to claim 43, wherein the processor further includes means to determine a percentage of said amount of charge supplied to the battery since the most recent one of said intervals.

45. A combination portable computer-rechargeable battery-battery recharger according to claim 44, wherein the means to determine said percentage includes means to determine said percentage based on battery temperature and battery current.

46. A combination portable computer-rechargeable battery-battery recharger according to

-114-

claim 45, wherein the means to determine said percentage includes:

a look-up table having a multitude of values stored therein; and

means to select one of said values based on battery temperature and battery current.

47. A combination portable computer-rechargeable battery-battery recharger according to claim 45, wherein:

at each of said intervals,

the processor determines the amount of current internally discharged by the battery since the most recent previous one of said intervals.

48. A combination portable computer-rechargeable battery-battery recharger according to claim 45, wherein:

said stored values further include a full capacity value representing a full capacity of the battery;

the processor periodically resets said full capacity value; and

the processor calculates the remaining capacity of the battery according to the equation

$$CAP_{REM} = CAP_{FC} - \Sigma_d - \Sigma_s + \Sigma_c$$

where:  $CAP_{REM}$  is the remaining capacity of the battery,

$CAP_{FC}$  is the most recently reset value for the full capacity value,

-115-

$\Sigma_d$  is the amount of charge internally discharged in the battery since the full capacity value of the battery was most recently reset,

$\Sigma_c$  is the amount of charge discharged by the battery since the full capacity value was most recently reset, and

$\Sigma_c$  is a percentage of the amount of charge supplied to the battery since the full capacity was most recently reset.

49. A combination portable computer-rechargeable battery-battery recharger according to claim 48, wherein:

the processor makes a series of calculations at regular intervals, said series of calculation including,

for each of said intervals

i) calculating the amount of charge internally discharged in the battery during the interval,

ii) if the battery is in the discharge mode, calculating the amount of charge discharged by the battery during the interval, and

iii) if the battery is in the charge mode, calculating the amount of charge supplied to the battery during the interval.

50. A combination portable computer-rechargeable battery-battery recharger according to claim 49, wherein:

-116-

$\Sigma_d$  is the summation of the amounts of charge internally discharged in the battery during the intervals since the full capacity of the battery was most recently reset;

$\Sigma_s$  is the summation of the amounts of charge discharged by the battery during the intervals since the full capacity of the battery was most recently reset; and

$\Sigma_c$  is a percentage of the summation of the amounts of charge supplied to the battery since the full capacity of the battery was most recently reset.

51. A combination portable computer-rechargeable battery-battery recharger according to Claim 48, wherein said percentage is based on battery temperature and battery current.

-117-

52. A battery system having power management capabilities, and comprising:

First and second terminal means for connecting the battery system to a battery powered device and to a battery recharger;

a battery including at least one rechargeable battery connected to the first and second terminal means, said battery having

i) a discharge mode for supplying electrical power to the first and second terminal means and to the battery powered device, and

ii) a charge mode for receiving electrical power from the first and second terminal means;

sensing means for sensing and generating analog signals representing battery voltage, battery temperature, and current at said first and second terminal means;

an integrated circuit including

i) an analog-to-digital converter for receiving said analog signals and converting said analog signals to digital signals representing battery voltage, battery temperature, and current at said first and second terminal means, and

ii) a processor connected to the analog-to-digital converter for receiving the digital signals therefrom, and for performing predefined calculations using said digital signals,

-118-

a data bus for transmitting data between the processor and the battery powered device;

wherein the integrated circuit comprises a multitude of layers, said multitude of layers including upper and lower layers,

wherein said lower layers form a random access memory area for storing a plurality of variable data values, said plurality of variable data values including data values representing battery voltage, battery temperature and current at said first and second terminal means;

wherein said upper layers form a read only memory area for storing a plurality of fixed data values.

53. A battery system according to Claim 52, wherein the upper layers are formed using a metal mask.

54. A battery system according to Claim 52, wherein said fixed data values include a unique battery identification code.

55. A battery system according to Claim 52, wherein the read only memory area contains a plurality of fixed algorithms.

56. A battery system according to Claim 52, for use by a customer having a need for a specific algorithm, and wherein:

the read only memory area stores said specific algorithm.



-119-

57. A battery system according to Claim 52, wherein:

each of the upper layers includes a matrix consisting of  $n$  rows and  $m$  columns, the rows and columns intersecting to form  $n \times m$  matrix locations; and

a respective one transistor is located at each one of the matrix locations.

58. A battery system according to Claim 57, wherein:

each of the upper layers further includes a plurality of common lines having a common electrical voltage level;

each of the transistors includes a source terminal and a drain terminal;

the source terminals of selected transistors are directly connected to the drain terminals of other transistors; and

the source and drain terminals of other selected transistors are both directly connected to one of the common lines.

59. A battery system according to Claim 58, wherein:

the transistors in each of said upper layers consist of first and second groups of transistors;

the source terminals of the transistors of the first group are directly connected to the drain terminals of others of the transistors; and

-120-

the source and drain terminals of the transistors of the second group are directly connected to one of the common lines.

60. A battery system according to Claim 58, wherein the source and drain terminals of each one of said other selected transistors are both directly connected to the same one of the common lines.

1

## AMENDED CLAIMS

[received by the International Bureau on 26 April 1996(26.04.96);  
original claims 1 - 60 replaced by amended claims 1 - 175 (83 pages)]

5

1. A battery pack comprising:

terminal means for connecting the battery  
pack to a battery powered device;

a battery including at least one  
rechargeable battery cell connected to the terminal  
10 means, said battery having

i) a discharge mode for supplying  
electrical power to the battery powered device, and  
ii) a charge mode for receiving electrical  
15 power from the terminal means;

sensing means for sensing and generating  
analog signals representing battery voltage, battery  
temperature, and battery current;

an analog-to-digital converter having abled  
20 and disabled states, wherein in the abled state, the  
converter receives said analog signals and converts  
said analog signals to digital signals representing  
battery voltage, battery temperature, and battery  
current;

25

a memory area for storing data values  
including at least values representing battery  
voltage, battery temperature and battery current; and

a processor connected to the analog-to-  
30 digital converter for receiving the digital signals.

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1 therefrom, and for performing a predefined series of  
calculations using said digital signals;

wherein the processor has (i) a normal mode,  
(ii) a standby mode, and (iii) a sleep mode,

5 in the normal mode, the processor performs  
said series of calculations at first regular cycles,  
in the standby mode, the processor performs  
said series of calculations at second regular cycles,  
said second cycles being longer than said first  
10 cycles, and

in the sleep mode, the processor does not  
perform said series of calculations, and the processor  
places the analog-to-digital converter in the disabled  
mode; and

15 wherein, the processor enters the standby  
mode when the battery current falls below a preset  
current level, the processor enters the sleep mode  
when the battery voltage falls below a preset voltage  
20 level, and the processor enters the normal mode when  
the battery voltage rises above a predetermined  
voltage level.

2. A battery pack according to Claim 1,  
wherein the battery has a variable capacity, and said  
25 series of calculations includes calculating a value  
representing remaining capacity of the battery.

3. A battery pack according to Claim 1,  
wherein:

30 the battery has a nominally fully discharged  
voltage value;

35

-123-

1 the memory area receives operating power  
from the battery and requires a minimum operating  
voltage to maintain said stored data values; and  
said minimum operating voltage is below said  
5 nominally fully discharged voltage value, wherein the  
memory area maintains said stored data values even  
when the battery is nominally fully discharged.

4. A battery pack according to Claim 1,  
wherein:

10 the length of each of the second cycles is  
an integer multiple of the length of each of the first  
cycles.

5. A battery pack according to Claim 1,  
15 wherein the analog-to-digital converter, the  
processor, and the memory area receive operating power  
from the battery.

6. A battery pack according to Claim 1,  
further including:

20 data receiving means to receive data from  
the battery powered device, said receiving means  
having an abled state and a disabled state;

in the abled state, the receiving means is  
able to receive data from the battery powered device;  
25 and

in the disabled state, the receiving means  
is disabled from receiving data from the battery  
powered device.

30

35

- 1                   7. A battery pack according to Claim 6,  
      wherein:  
          each of the first cycles includes first and  
          second intervals; and  
5           during each of the first intervals of the  
      first cycles, the processor (i) performs said series  
      of calculations, and (ii) places the receiving means  
      in the disabled state to inhibit the transmission of  
      data to the processor from the battery powered device  
10       while the processor is performing said calculations.
8. A battery pack according to Claim 1,  
      wherein the processor performs additional  
      calculations, said additional calculations including  
15       calculating a value representing a learned full charge  
      capacity of the battery.
9. A battery pack according to Claim 1,  
      further comprising:  
          a comparator circuit connected to the  
20       sensing means to receive the analog signal  
      representing battery voltage, and to generate a wake-  
      up signal, and to transmit the wake-up signal to the  
      processor, when the battery voltage is above the  
      predetermined voltage level; and  
25       wherein the processor enters the normal mode  
      when the processor receives the wake-up signal from  
      the comparator circuit.
10. A battery pack according to Claim 1,  
30       further comprising a switching network connected to  
      the sensing means and to the analog-to-digital

-125-

- 1 converter, for receiving the analog signals from the sensing means and transmitting the analog signals, one at a time, to the analog-to-digital converter.
- 5 11. A battery pack comprising:  
terminal means for connecting the battery pack to a battery powered device;  
a battery including at least one rechargeable battery cell connected to the terminal means, said battery having
- 10 i) a discharge mode for supplying electrical power to the battery powered device, and  
ii) a charge mode for receiving electrical power from the terminal means;
- 15 sensing means for sensing and generating analog signals representing battery voltage, battery temperature, and battery current;  
an analog-to-digital converter having abled and disabled states, wherein in the abled state, the
- 20 converter receives said analog signals and converts said analog signals to digital signals representing battery voltage, battery temperature, and battery current;
- 25 a memory area for storing data values including at least values representing battery voltage, battery temperature and battery current;  
an internal oscillator for generating internal clock signals at a first frequency,
- 30 a processor connected to the analog-to-digital converter for receiving the digital signals

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-126-

1 therefrom, and for performing a predefined series of  
calculations using said digital signals;

wherein each of said calculations includes a  
series of timed steps, and the timing of said steps is  
5 controlled by the clock signals from the internal  
oscillator;

an external oscillator for generating clock  
signals at a second frequency; and

10 means connecting the external oscillator to  
the processor to transmit to the processor the clock  
signals from the external oscillator;

wherein the processor performs said series  
of calculations at regular cycles, each of said cycles  
being started by receipt by the processor of one of  
15 the clock signals from the external processor.

12. A battery pack according to Claim 11,  
wherein:

the processor has normal and standby modes;  
20 in the normal mode, the processor performs  
said series of calculations at first regular cycles,  
and in the standby mode, the processor performs said  
series of calculations at second regular cycles; and  
each of the first and second cycles is  
25 started by receipt of the processor of one of the  
clock signals from the external processor.

13. A battery pack according to Claim 11,  
wherein:

30 the processor has normal and sleep modes;

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-127-

1           in the normal mode, the processor performs  
said series of calculations;

          in the sleep mode, the processor does not  
perform said series of calculations;

5           the battery pack further includes a  
comparator circuit connected to the sensing means to  
receive the analog signal representing battery  
voltage, and connected to the external oscillator to  
receive the clock signals therefrom;

10           when the comparator circuit receives the  
clock signals from the external oscillator, the  
comparator circuit generates a wake-up signal and  
transmits the wake-up signal to the processor, if the  
15 battery voltage is above a predetermined level; and

          the processor enters the normal mode when  
the processor receives the wake-up signal from the  
comparator circuit.

          14. A battery pack according to Claim 11,  
20 further including data receiving means to receive data  
from the battery powered device, said receiving having  
an abled state and a disabled state;

          in the abled state, the receiving means is  
able to receive data from the battery powered device;  
25 and

          in the disabled state, the receiving means  
is disabled from receiving data from the battery  
powered device;

30           each of the said regular cycles includes  
first and second intervals; and

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-128-

1 during each of the first intervals of said  
regular cycles, the processor (i) performs said series  
of calculations, and (ii) places the receiving means  
in the disabled state to inhibit the transmission of  
5 data to the processor from the battery powered device  
while the processor is performing said calculations.

15. A battery pack comprising:  
terminal means for connecting the battery  
pack to a battery powered device;  
10 a battery including at least one  
rechargeable battery cell connected to the terminal  
means, said battery having

i) a discharge mode for supplying  
15 electrical power to the battery powered device, and  
ii) a charge mode for receiving electrical  
power from the terminal means;

sensing means for sensing and generating  
analog signals representing battery voltage, battery  
20 temperature, and battery current;

an analog-to-digital converter having abled  
and disabled states, wherein in the abled state, the  
converter receives said analog signals and converts  
said analog signals to digital signals representing  
25 battery voltage, battery temperature, and battery  
current;

a memory area for storing data values  
including at least values representing battery  
30 voltage, battery temperature and battery current;

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-129-

1           an internal oscillator for generating  
internal clock signals at a first frequency,  
a processor connected to the analog-to-  
digital converter for receiving the digital signals  
5   therefrom, and for performing a predefined series of  
calculations using said digital signals;  
wherein each of said calculations includes a  
series of timed steps, and the timing of said steps is  
controlled by the clock signals from the internal  
10   oscillator;  
an external oscillator for generating clock  
signals at a second frequency; and  
means connecting the external oscillator to  
15   the processor to transmit to the processor the clock  
signals from the external oscillator; and  
wherein the processor has (i) a normal mode,  
(ii) a standby mode, and (iii) a sleep mode,  
in the normal mode, the processor performs  
20   said series of calculations at first regular cycles,  
each of said first cycles being started by receipt by  
the processor of one of the clock signals from the  
external processor,  
in the standby mode, the processor performs  
25   said series of calculations at second regular cycles,  
said second cycles being longer than said first  
cycles, each of said second cycles also being started  
by receipt by the processor of one of the clock  
30   signals from the external processor, and

35

-130-

1           in the sleep mode, the processor does not  
perform said series of calculations, and the processor  
places the analog-to-digital converter in the disabled  
mode; and

5           wherein the processor enters the standby  
mode when the battery current fall below a preset  
current level, the processor enters the sleep mode  
when the battery voltage falls below a preset voltage  
level, and the processor enters the normal mode when  
10 the battery voltage rises above a predetermined level.

16. A battery pack according to Claim 15,  
further including:

15           a comparator circuit connected to the  
sensing means to receive the analog signal  
representing battery voltage, and to generate a wake-  
up signal, and to transmit the wake-up signal to the  
processor, when the battery voltage is above the  
predetermined level; and

20           wherein the processor enters the normal mode  
when the processor receives the wake-up signal from  
the comparator circuit.

17. A battery pack according to Claim 16,  
25 further comprising a switching network connected to  
the sensing means and to the analog-to-digital  
converter for receiving the analog signals from the  
sensing means and transmitting the analog signals, one  
at a time, to the analog-to-digital converter.

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-131-

1 18. A battery pack according to Claim 15,  
further including data receiving means to receive data  
from the battery powered device, and wherein:

5 said receiving means has an abled state and  
a disabled state;

in the abled state, the receiving means is  
able to receive data from the battery powered device;

10 in the disabled state, the receiving means  
is disabled from receiving data from the battery  
powered device;

each of the first cycles includes first and  
second intervals; and

15 during each of the first intervals of the  
first cycles, the processor (i) performs said series  
of calculations, and (ii) places the receiving means  
in the disabled state to inhibit the transmission of  
data to the processor from the battery powered device  
while the processor is performing said calculations.

20 19. A method of operating a battery system  
having a rechargeable battery and a processor, the  
method comprising:

25 sensing, and generating analog signals  
representing, battery voltage, battery temperature and  
battery current;

converting said analog signals to digital  
signals representing battery voltage, battery  
temperature and battery current;

30 storing data values in a memory area, said  
stored data values including at least values

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-132-

1 representing battery voltage, battery temperature and  
battery current;

the processor performing a series of  
predefined calculations using said digital values;

5 wherein the processor has (i) a normal mode,  
(ii) a standby mode, and (iii) a sleep mode;

in the normal mode, the processor performs  
said series of predefined calculations at first  
regular cycles; in the standby mode, the processor  
10 performs said series of predefined calculations at  
second regular cycles; and in the sleep mode, the  
processor does not perform said series of  
calculations;

15 the processor (i) entering the standby mode  
when the battery current falls below a preset current  
level, (ii) entering the sleep mode when the battery  
voltage falls below a preset voltage level, and (iii)  
entering the normal mode when the battery voltage is  
20 above a predetermined voltage level.

20. A method according to Claim 19, wherein  
the step of converting the analog signals representing  
battery voltage, battery temperature and battery  
current to digital signals includes the steps of  
25 transmitting said analog signals, one at a time, to an  
analog-to-digital converter to convert said analog  
signals to said digital signals.

21. A method according to Claim 20, wherein  
the analog-to-digital converter has (i) an abled state  
30 to convert said analog signals to said digital

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-133-

1 signals, and (ii) a disabled state, and wherein the  
step of the processor entering the sleep mode includes  
the step of placing the analog-to-digital converter in  
the disabled state when the processor enters the sleep  
5 mode.

22. A method according to Claim 19, wherein  
the step of the processor entering the normal mode  
includes the steps of:

10 comparing the battery voltage to the  
predetermined voltage level at predefined intervals;  
generating a wake-up signal when the battery  
voltage is above said predetermined voltage level;  
transmitting the wake-up signal to the  
15 processor; and  
the processor entering the normal mode in  
response to transmitting the wake-up signal to the  
processor.

23. A method according to Claim 19, wherein  
20 each of the first cycles has first and second  
intervals and the battery system further includes a  
data receiving means, and wherein:

the step of performing the predefined  
calculations includes the step of performing the  
25 predefined calculations in the first interval of each  
of the first cycles; and

the method further includes the steps of  
i) transmitting data to the data receiving  
30 means, and

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-134-

1           ii) disabling the data receiving means  
during the first interval of each of the first cycles  
to inhibit the transmission of data to the data  
receiving means while the processor is performing the  
5 predefined calculations.

24. A method of operating a battery system  
having a rechargeable battery, a processor, and first  
and second oscillators for generating clock signals at  
first and second frequencies, the method comprising:  
10           sensing, and generating analog signals  
representing, battery voltage, battery temperature and  
battery current;

          converting said analog signals to digital  
signals representing battery voltage, battery  
15 temperature and battery current;

          storing data values in a memory area, said  
stored data values including at least values  
representing battery voltage, battery temperature and  
20 battery current;

          the processor performing a series of  
predefined calculations at regular cycles using said  
digital values, each of said calculations including a  
series of timed steps;

25           transmitting the clock signals from the  
first and second oscillators to the processor;

          starting each of said regular cycles in  
response to transmission to the processor of one of  
30 the clock signals from the first oscillator; and

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-135-

1 controlling the timing of the timed steps of  
the predetermined calculations using the clock signals  
from the second oscillator.

5 25. A method according to Claim 24, wherein:  
the processor has normal and standby modes;  
the step of performing the series of  
predefined calculations includes the steps of

10 i) performing said series of calculations at  
first regular cycles when the processor is in the  
normal mode, and

ii) performing said series of calculations  
at second regular cycles when the processor is in the  
standby mode; and

15 the step of starting each of said regular  
cycles includes the step of starting each of said  
first regular cycles and each of said second regular  
cycles in response to transmission to the processor of  
one of the clock signals from the first oscillator.

20 26. A method according to Claim 24, wherein  
the step of converting the analog signals representing  
battery voltage, battery temperature and battery  
current to digital signals includes the steps of  
transmitting said analog signals, one at a time, to an  
25 analog-to-digital converter to convert said analog  
signals to said digital signals.

30 27. A method according to Claim 24, wherein:  
the processor has normal and sleep modes;  
in the normal mode, the processor performs  
said series of calculations;

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-136-

1           in the sleep mode, the processor does not  
perform said series of calculations; and  
the method includes the further step of the  
processor entering the normal mode when the battery  
5 voltage is above a predetermined voltage level.

28. A method according to Claim 27, wherein  
the step of the processor entering the normal mode  
includes the steps of:

10           comparing the battery voltage to the  
predetermined voltage level at predefined intervals;  
generating a wake-up signal when the battery  
voltage is above said predetermined voltage level;  
transmitting the wake-up signal to the  
15 processor; and  
the processor entering the normal mode in  
response to transmitting the wake-up signal to the  
processor.

29. A method according to Claim 28, wherein  
20 the battery system further includes a voltage  
comparator, and wherein:

the comparing step includes the steps of  
transmitting the clock signals from the first  
oscillator to the voltage comparator to activate the  
25 voltage comparator at said defined intervals to  
compare the battery voltage to the predetermined  
voltage level; and

the generating step includes the step of the  
30 voltage comparator generating the wake-up signal when

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AMENDED SHEET (ARTICLE 19)

-137-

1 the battery voltage is above the predetermined voltage level.

5 30. A method according to Claim 24, wherein:  
the processor has normal and sleep modes;  
in the normal mode, the processor performs  
said series of calculations;

in the sleep mode, the processor does not  
perform said series of calculations;

10 the method further includes the steps of  
1) the processor entering the sleep mode  
when the battery voltage falls below a preset voltage  
level, and

15 11) disabling the second oscillator when the  
processor enters the sleep mode to inhibit the second  
oscillator from generating clock signals when the  
battery voltage falls below the preset voltage level.

20 31. A method according to Claim 24, further  
including the step of the processor performing  
additional calculations at predefined times, said  
additional calculations including calculating a value  
representing a learned full charge capacity of the  
battery.

25 32. A method of operating a battery system  
having a rechargeable battery, a processor, and first  
and second oscillators for generating clock signals at  
first and second frequencies, the method comprising:  
sensing, and generating analog signals  
30 representing, battery voltage, battery temperature and  
battery current;

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AMENDED SHEET (ARTICLE 19)

-138-

- 1           converting said analog signals to digital  
signals representing battery voltage, battery  
temperature and battery current;  
          storing data values in a memory area, said  
5 stored data values including at least values  
representing battery voltage, battery temperature and  
battery current;  
          the processor performing a series of  
predefined calculations using said digital values,  
10 each of said calculations including a series of timed  
steps;  
          controlling the timing of the timed steps  
using the clock signals from the first oscillator;  
          wherein the processor has (i) a normal mode,  
15 (ii) a standby mode, and (iii) a sleep mode;  
          in the normal mode, the processor performs  
said series of predefined calculations at first  
regular cycles; in the standby mode, the processor  
20 performs said series of predefined calculations at  
second regular cycles; and in the sleep mode, the  
processor does not perform said series of  
calculations;  
          transmitting the clock signals from the  
25 second oscillator to the processor;  
          each of the first and second cycles starting  
in response to transmission to the processor of one of  
the clock signals from the second oscillator; and  
30           the processor (i) entering the standby mode  
when the battery current falls below a preset current

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-139-

1 level, (ii) entering the sleep mode when the battery  
voltage falls below a preset voltage level, and (iii)  
entering the normal mode when the battery voltage is  
above a predetermined voltage level.

5 33. A method according to Claim 32, wherein  
the step of the processor entering the normal mode  
includes the steps of:

comparing the battery voltage to the  
predetermined voltage level at predefined intervals;  
10 generating a wake-up signal when the battery  
voltage is above said predetermined voltage level;  
transmitting the wake-up signal to the  
processor; and  
15 the processor entering the normal mode in  
response to transmitting the wake-up signal to the  
processor.

34. A method according to Claim 33, wherein  
the battery system further includes a voltage  
20 comparator, and wherein:

the comparing step includes the steps of  
transmitting the clock signals from the second  
oscillator to the voltage comparator to activate the  
voltage comparator at said defined intervals to  
25 compare the battery voltage to the predetermined  
voltage level; and

the generating step includes the step of the  
voltage comparator generating the wake-up signal when  
30 the battery voltage is above the predetermined voltage  
level.

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AMENDED SHEET (ARTICLE 19)

-140-

1           35. A method according to Claim 32, wherein  
the step of entering the sleep mode includes  
the step of disabling the first oscillator when the  
processor enters the sleep modes to inhibit the first  
5 oscillator from generating clock signals when the  
battery voltage falls below the preset voltage level.

10           36. A method according to Claim 32, wherein  
the battery has a variable capacity, and said  
predefined calculations include calculating a value  
representing remaining battery capacity of the  
battery.

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-141-

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37. A battery pack comprising:

terminal means for connecting the battery  
pack to a battery powered device and to a battery

5 recharger;

a battery including at least one  
rechargeable battery cell connected to the terminal  
means, said battery having

10 i) a discharge mode for supplying  
electrical power to the battery powered device, and  
ii) a charge mode for receiving electrical  
power from the terminal means;

15 sensing means for sensing and generating  
analog signals representing battery voltage, battery  
temperature, and battery current;

20 an analog-to-digital converter for receiving  
said analog signals and converting said analog signals  
to digital signals representing battery voltage,  
battery temperature, and battery current;

25 a processor connected to the analog-to-  
digital converter for receiving the digital signals  
therefrom, and for performing a predefined series of  
calculations using said digital signals;

a memory area for storing data values  
including at least values representing battery  
voltage, battery temperature and battery current;

30 means to supply electrical power to said  
memory area, including a capacitor connected to the

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-142-

1 battery to receive electrical power therefrom, and  
connected to the memory area to supply electrical  
power thereto.

5 38. A battery pack according to Claim 37,  
wherein:

the means to supply electrical power to said  
memory area further includes a power supply circuit  
electrically connecting the memory area to the battery  
to supply electrical power to the memory area; and  
10 the memory area receives electrical power  
from the capacitor in case of an interruption in the  
supply of electrical power to the memory area through  
the power supply circuit.

15 39. A battery pack according to Claim 38,  
wherein the power supply circuit includes a delatching  
subcircuit for electrically decoupling the memory area  
from the battery under predetermined conditions.

20 40. A battery pack according to Claim 39,  
further including an internal power terminal; and  
wherein the power supply circuit includes:

means electrically connecting the battery  
to said power terminal to supply electrical power to  
said power terminal from the battery; and  
25 means electrically connecting the power  
terminal to the memory area to supply electrical power  
to said memory area from the power terminal.

30 41. A battery pack according to Claim 40,  
wherein the delatching circuit electrically decouples  
the memory area from the power terminal when the

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-143-

1 voltage of the power terminal falls below a given level.

42. A battery pack according to Claim 41, wherein:

5 the delatching circuit includes

i) a switching transistor located in the means electrically connecting the power terminal to the memory area,

10 ii) a sensor for sensing, and for generating a signal representing, the voltage of the power terminal, and

15 iii) means for applying to the switching transistor the signal representing the voltage of the power terminal;

the switching transistor has

i) a conductive state for electrically coupling the memory area to the power terminal, and

20 ii) a non-conductive state for electrically decoupling said memory area from the power terminal; and

25 the switching transistor switches from the conductive state to the non-conductive state when the voltage of the power terminal falls below the given level.

43. A battery pack according to Claim 37, wherein the terminal means includes first and second terminals and wherein the battery pack further  
30 includes means to inhibit the flow of current through the battery in case of a short circuit across the

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-144-

1 first and second terminal, and to help maintain the  
flow of current from the battery to the memory area in  
case of said short circuit.

44. A battery pack according to Claim 43,  
5 wherein the means to inhibit the flow of current  
through the battery includes a fuse located in series  
between the battery cell and one of the terminals.

45. A battery pack according to Claim 43,  
10 wherein the means to inhibit the flow of current  
through the battery includes a positive temperature  
coefficient element located in series between the  
battery cell and one of the terminals, for creating a  
high impedance between the battery cell and said one  
15 of the terminals in case of said short circuit.

46. A battery pack according to Claim 43,  
wherein:

in case of an interruption of the supply of  
electrical power to the memory area from the battery,  
20 said memory area receives electrical power from the  
capacitor for at least a given period of time; and

in case of a short circuit across the first  
and second terminals, the means to inhibit the flow of  
current through the battery raises the voltage of the  
25 battery above said preset level within said given  
period of time.

47. A battery according to Claim 37,  
wherein:

30 the battery has a variable capacity; and  
said series of calculations include

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-145-

- 1           1) calculating a value representing  
remaining capacity of the battery, and  
          11) calculating a value representing learned  
capacity of the battery.
- 5           48. A method of operating a battery system  
having a rechargeable battery, a processor and a  
memory area, the method comprising:  
          sensing, and generating analog signals  
10       representing, battery voltage, battery temperature and  
battery current;  
          converting said analog signals to digital  
signals representing battery voltage, battery  
temperature and battery current;  
15       storing data values in the memory area, said  
stored data values including at least values  
representing battery voltage, battery temperature and  
battery current;  
          the processor performing a series of  
20       predefined calculations using said digital values;  
          conducting electrical current from the  
battery to a capacitor to develop an electric voltage  
level therein; and  
          electrically coupling the capacitor to the  
25       memory area to conduct electrical power thereto,
49. A method according to Claim 48, further  
including the step of conducting electrical current  
from the battery to the memory area, via a power  
30       supply circuit; and wherein in case of an interruption  
of the supply of electrical current from the battery

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AMENDED SHEET (ARTICLE 19)

-146-

1 to the memory area via the power supply circuit, said  
memory area receives electrical power from the  
capacitor.

50. A method according to Claim 49, further  
5 including the step of electrically decoupling the  
memory area from the battery under predetermined  
conditions.

51. A method according to Claim 50, wherein  
the step of electrically decoupling the memory area  
10 from the battery includes the steps of:

sensing voltage in the power supply circuit;

and

15 electrically decoupling the memory area from  
the battery when the sensed voltage in the power  
supply circuit falls below a given level.

52. A method according to Claim 51, wherein  
the battery system includes an integrated circuit, the  
processor and the memory area are part of the  
20 integrated circuit, and the integrated circuit further  
includes a power terminal, and wherein the step of  
conducting electrical current from the battery to the  
memory area includes the steps of:

25 electrically coupling the power terminal to  
the battery to produce a voltage level at the power  
terminal; and

30 electrically coupling the power terminal to  
the memory area to apply to said memory area the  
voltage level at the power terminal.

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-147-

1                   53. A method according to Claim 52,  
                  wherein:

                  the step of sensing voltage in the power  
                  supply circuit includes the step of sensing the  
5   voltage level at said power terminal; and  
                  the step of decoupling the memory area from  
                  the battery when the sensed voltage in the power  
                  supply circuit falls below a given voltage level  
                  includes the step of electrically decoupling the  
10   memory area from the power terminal when the voltage  
                  level at said power terminal falls below the given  
                  level.

                  54. A method according to Claim 48, wherein  
15   the battery system further includes first and second  
                  terminals and the rechargeable battery is connected to  
                  said terminals to supply electrical power to a battery  
                  powered device, and wherein the method further  
                  includes the step of

20                   inhibiting the flow of current through the  
                  battery in case of a short circuit across the first  
                  and second terminals to help maintain the flow of  
                  current from the battery to the memory area in case of  
                  said short circuit.

25                   55. A method according to Claim 54,  
                  wherein:

                  the step of inhibiting the flow of current  
                  through the battery includes the step of raising the  
30   voltage of the battery above said predetermined  
                  voltage level within a given period of time; and

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-148-

1           the step of electrically coupling the  
capacitor to the memory area includes the step of, in  
case of said short circuit, conducting electrical  
power from the capacitor to the memory area to  
5 maintain a voltage level at the memory area above a  
predetermined voltage level for at least a given  
period of time.

56. A method according to Claim 48, wherein  
the battery has a nominally fully discharged voltage  
10 value, and the memory area requires a minimum  
operating voltage to maintain said stored data values,  
said minimum operating voltage being below said  
nominally fully discharged voltage, and wherein the  
15 method further comprises the step of  
when the battery voltage is below the  
nominally fully discharged voltage value, applying a  
voltage to the memory area that is above said minimum  
operating voltage to maintain said stored data values.  
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-149-

- 1           57. A battery pack comprising:  
terminal means for connecting the battery  
pack to a battery powered device and to a battery  
recharger;
- 5           a battery including at least one  
rechargeable battery cell connected to the terminal  
means, said battery having
- 10           i) a discharge mode for supplying  
electrical power to the battery powered device, and  
ii) a charge mode for receiving electrical  
power from the terminal means;
- 15           sensing means for sensing and generating  
analog signals representing battery voltage, battery  
temperature, and battery current;
- 20           an analog-to-digital converter for receiving  
said analog signals and for converting both positive  
and negative analog signals to digital signals  
representing battery voltage, battery temperature, and  
battery current;
- 25           a processor connected to the analog-to-  
digital converter for receiving the digital signals  
therefrom, and for performing a predefined series of  
calculations using said digital signals; and
- 30           a memory area for storing data values  
including at least values representing battery  
voltage, battery temperature and battery current.
- 35

-150-

1           58. A battery pack according to Claim 57,  
wherein the analog-to-digital converter includes:

          a bandgap reference circuit to provide a  
preset analog voltage; and

5           a voltage shifting circuit to provide a  
variable base reference voltage to facilitate  
generating digital values representing positive and  
negative analog signals.

10           59. A battery pack according to Claim 58,  
wherein the analog-to-digital converter further  
includes a voltage divider network to receive the  
preset analog voltage from the bandgap reference  
circuit and to divide said preset analog voltage into  
15 a plurality of voltage output values.

          60. A smart battery according to Claim 58,  
wherein the analog-to-digital converter further  
includes a sigma-delta converter for receiving the  
analog signals from the sensing means and for  
20 converting said analog signals to digital values  
representing battery voltage, battery temperature, and  
battery current.

          61. A battery pack according to Claim 57,  
wherein the analog-to-digital converter processes each  
25 of the analog signals representing battery voltage,  
battery temperature, and battery current for a  
respective period to produce the digital values  
representing battery voltage, battery temperature, and  
30 battery current.

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-151-

1           62. A battery pack according to Claim 61,  
further including:

an oscillator for generating clock signals  
at a given frequency; and

5           means to transmit said clock signals to the  
analog-to-digital converter; and

wherein each of said periods has a length  
determined by said clock signals.

10          63. A smart battery pack according to Claim  
62, wherein:

the analog-to-digital converter processes  
the analog signals representing battery voltage,  
battery temperature, and battery current for first,  
15          second and third periods respectively; and

the lengths of said first, second and third  
periods are determined by the lengths of time required  
for the analog-to-digital converter to receive,  
respectively, first, second and third numbers of the  
20          clock signals.

64. A battery pack according to Claim 58,  
wherein the voltage shifting circuit includes:

a first capacitor having first and second  
opposite sides;

25          means to generate a reference ground voltage  
level; and

a switching network for applying the  
reference ground voltage level and the analog signals  
to the first and second sides of the capacitor to  
30          develop a voltage level at the capacitor;

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-152-

- 1 the switching network having
- 1) a first state for applying the reference  
ground voltage level to the first side of the  
capacitor, and for applying at least one of said  
5 analog signals to the second side of the capacitor,  
and
- ii) a second state for applying the  
reference ground voltage level to the second side of  
the capacitor, and for applying at least one of said  
10 analog signals to the first side of the capacitor.
65. A battery pack according to Claim 64,  
wherein:
- the analog-to-digital converter further  
15 includes a sigma-delta converter including
- i) means to generate a second reference  
voltage level,
- ii) an integrator having first and second  
inputs,
- 20 iii) means to apply the second reference  
voltage level to the first input of the integrator,  
and
- iv) a switch electrically located in series  
between the first capacitor and the second input of  
25 the integrator; and
- the switch has
- i) a conductive state for applying the  
voltage level of the first capacitor to the second  
30 input of the integrator, and

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-153-

1           ii) a non-conductive state for electrically  
decoupling the first capacitor from the second input  
of the integrator.

5           66. A battery pack according to Claim 64,  
wherein the sigma-delta converter further includes:  
a second capacitor electrically located in  
parallel with the integrator; and  
a further switch electrically located in  
parallel with the second capacitor to selectively  
10 discharge said second capacitor.

67. A battery pack according to Claim 64,  
wherein:  
the integrator has an output voltage level;  
the sigma-delta converter further includes  
15 v) a comparator having first and second  
inputs,

vi) means to apply the second reference  
voltage level to the first input of the comparator,  
20 and

vii) means to apply the output voltage level  
of the integrator to the second input of the  
comparator; and

25           the comparator has  
i) a first output when the voltage level  
applied to the first input of the comparator is less  
than the voltage level applied to the second input of  
the comparator, and

30           ii) a second output when the voltage level  
applied to the first input of the comparator is

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-154-

1 greater than the voltage level applied to the second  
input of the comparator.

68. A battery pack according to Claim 67,  
wherein:

5 the sigma-delta converter further includes  
vii) a counter, and

ix) means for applying the output of the  
comparator to the counter; and

10 the counter maintains a count of the number  
of times the first output of the comparator is applied  
to the counter during a defined period of time.

69. An analog-to-digital converter  
including:

15 input means to receive positive and  
negative analog input signals;

a signal converter to receive the analog  
signals from the input means and for converting both  
positive and negative analog signals to digital

20 signals; and

output means for receiving the digital  
signals from the converter means and transmitting the  
digital signals from the analog-to-digital converter.

25 70. An analog-to-digital converter according  
to Claim 69, wherein the signal converter includes:

a bandgap reference circuit to provide a  
preset analog voltage; and

30 a voltage shifting circuit to provide a  
variable base reference voltage to facilitate

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-155-

1 generating digital values representing positive and negative analog signals.

71. An analog-to-digital converter according to Claim 70, wherein the signal converter  
5 further includes a voltage divider network to receive the preset analog voltage from the bandgap reference circuit and to divide said preset analog voltage into a plurality of voltage output values.

72. An analog-to-digital converter according to Claim 69, wherein:  
10

the input means receives a plurality of different types of input signals; and

the signal converter further includes a  
15 sigma-delta converter to receive said different types of input signals and to process the different types of input signals for different periods of time to produce digital signals representing the input signals.

73. An analog-to-digital converter according to Claim 72, wherein:  
20

the sigma-delta converter includes a clock input to receive clock input signals at defined frequencies; and

the different periods of time have lengths  
25 determined by the lengths of time required for the sigma-delta converter to receive different numbers of the clock signals.

74. An analog-to-digital converter according to Claim 70, wherein the voltage shifting circuit  
30 includes:

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-156-

- 1           a first capacitor having first and second  
opposite sides;  
          means to generate a reference ground voltage  
level; and
- 5           a switching network for applying the  
reference ground voltage level and the analog signals  
to the first and second sides of the capacitor to  
develop a voltage level at the capacitor;  
          the switching network having
- 10           i) a first state for applying the reference  
ground voltage level to the first side of the  
capacitor, and for applying analog signals to the  
second side of the capacitor, and
- 15           ii) a second state for applying the  
reference ground voltage level to the second side of  
the capacitor, and for applying the input signals to  
the first side of the capacitor.
- 20           75. An analog-to-digital converter according  
to Claim 74, wherein:  
          the signal converter further includes a  
sigma-delta converter including
- 25           i) means to generate a second reference  
voltage level,
- ii) an integrator having first and second  
inputs,
- iii) means to apply the second reference  
voltage level to the first input of the integrator,  
and
- 30

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-157-

1           iv) a switch electrically located in series  
between the first capacitor and the second input of  
the integrator; and

the switch has

5           1) a conductive state for applying the  
voltage level of the first capacitor to the second  
input of the integrator, and

10           ii) a non-conductive state for electrically  
decoupling the first capacitor from the second input  
of the integrator.

76. An analog-to-digital converter according  
to Claim 75, wherein the sigma-delta converter further  
includes:

15           a second capacitor electrically located in  
parallel with the integrator; and

          a further switch electrically located in  
parallel with the second capacitor to selectively  
discharge said second capacitor.

20           77. An analog-to-digital converter according  
to Claim 75, wherein:

the integrator has an output voltage level;  
the sigma-delta converter further includes

25           v) a comparator having first and second  
inputs,

vi) means to apply the second reference  
voltage level to the first input of the comparator,  
and

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-158-

- 1           vii) means to apply the output voltage level  
of the integrator to the second input of the  
comparator; and
- the comparator has
- 5           i) a first output when the voltage level  
applied to the first input of the comparator is less  
than the voltage level applied to the second input of  
the comparator, and
- ii) a second output when the voltage level  
10 applied to the first input of the comparator is  
greater than the voltage level applied to the second  
input of the comparator.
78. An analog-to-digital converter according  
15 to Claim 77, wherein:  
          the sigma-delta converter further includes  
          i) a counter, and  
          ii) means for applying the output of the  
comparator to the counter; and
- 20           the counter maintains a count of the number  
of times the first output of the comparator has been  
applied to the counter during a defined period of  
time.
79. A method of operating a battery system  
25 having a rechargeable battery, a processor, a memory  
area and an analog-to-digital converter, the method  
comprising:
- connecting the rechargeable battery to a  
30 battery powered device to supply electrical power  
thereto;



-159-

1       sensing, and generating analog signals  
representing, battery voltage, battery temperature and  
battery current, said analog signal including both  
positive and negative signals;

5       transmitting said analog signals to the  
analog-to-digital converter;

      the analog-to-digital converter, converting  
both the positive and negative analog signals to  
digital signals representing battery voltage, battery  
10      temperature and battery current; and

      storing data values in the memory area, said  
stored data values including at least values  
representing battery voltage, battery temperature and  
15      battery current.

      80. A method according to Claim 79, wherein  
the step of converting the analog signals to digital  
signals includes the steps of:

      generating a preset analog bandgap  
20      reference voltage; and

      generating a variable base reference voltage  
to facilitate generating digital values from both  
positive and negative analog current signals.

      81. A method according to Claim 80, wherein  
25      the step of generating the bandgap reference voltage  
includes the step of dividing the bandgap reference  
voltage into a plurality of output voltage values.

      82. A method according to Claim 81, wherein  
30      the step of converting the analog signals to digital  
signals further includes the steps of processing each

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-160-

1 of the analog signals representing battery voltage,  
battery temperature and battery current for a  
respective period of time to produce the digital  
values representing battery voltage, battery  
5 temperature and battery current.

83. A method according to Claim 82, further  
including the steps of:

generating clock signals at a given  
frequency;

10 transmitting the clock signals to the  
analog-to-digital converter; and

using the clock signals to determine the  
lengths of said periods of time.

15 84. A method according to Claim 80, wherein:  
the step of generating the base reference  
voltage includes the steps of generating a reference  
ground voltage level; and

the step of converting the analog signals to  
20 digital signals further includes the step of  
developing a voltage level in a capacitor having first  
and second opposite sides, including the steps of

i) at first times, applying the reference  
ground voltage level to the first side of the  
25 capacitor, and applying the analog signals to the  
second side of the capacitor; and

ii) at other times, applying the reference  
ground voltage level to the second side of the  
capacitor, and applying at least one of the analog  
30 signals to the first side of the capacitor.

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-161-

1           85. A method according to Claim 84, wherein  
the step of converting the analog signals to digital  
signals further includes the steps of:

          generating a second reference voltage level;  
5           applying the second reference voltage level  
to a first input of an integrator; and  
          selectively applying the voltage level of  
the capacitor to a second input of the integrator.

10           86. A method according to Claim 85,  
wherein:

          the integrator has an output voltage level;  
          the step of converting the analog signals to  
digital signals further includes the steps of

15           i) applying the second reference voltage  
level to a first input of a comparator, and  
          ii) applying the output voltage level of the  
integrator to a second input of the comparator;

          the comparator has a first output voltage  
20           level when the voltage level applied to the first  
input of the comparator is less than the voltage level  
applied to the second input of the comparator, and the  
comparator has a second output voltage level when the  
voltage level applied to the first input of the  
25           comparator is greater than the voltage level applied  
to the second input of the comparator; and

          the step of converting the analog signals to  
digital signals further includes the step of (iii)  
30           counting the number of times the comparator has the

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-162-

1 first output voltage level during a defined period of time.

87. A method of operating an analog-to-digital converter, comprising the steps of:

5 conducting both positive and negative analog signals to the converter; and

converting both the positive and negative analog signals to digital signals, including the steps of

10 i) generating a preset analog signal, and  
ii) generating a variable base reference signal to facilitate generating digital signals representing positive and negative analog signals.

15 88. A method according to Claim 87, wherein the step of converting the positive and negative analog signals includes the step of dividing the preset analog signal into a plurality of voltage output values.

20 89. A method according to Claim 87, wherein: the conducting step includes the step of conducting a plurality of different types of input signals to the converter; and

25 the step of converting the positive and negative analog signals further includes the step of processing the different types of input signals for different periods of time to produce digital signals representing the input signals.

30 90. A method according to Claim 89, wherein:

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-163-

1 the step of processing the different types  
of input signals includes the step of conducting clock  
signals to the converter at defined frequencies; and  
the different periods of time have length  
5 determined by the lengths of time required for the  
converter to receive different numbers of the clock  
signals.

91. A method according to Claim 87, wherein:  
the step of generating the base reference  
10 voltage includes the steps of generating a reference  
ground voltage level; and  
the step of converting the analog signals to  
digital signals further includes the step of  
developing a voltage level in a capacitor having first  
15 and second opposite sides, including the steps of  
i) at first times, applying the reference  
ground voltage level to the first side of the  
capacitor, and applying the analog signals to the  
20 second side of the capacitor, and  
ii) at other times, applying the reference  
ground voltage level to the second side of the  
capacitor, and applying at least one of the analog  
signals to the first side of the capacitor.  
25

92. A method according to Claim 91, wherein  
the step of converting the analog signals to digital  
signals further includes the steps of:  
generating a second reference voltage level;  
30 applying the second reference voltage level  
to a first input of an integrator; and

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-164-

1 selectively applying the voltage level of  
the capacitor to a second input of the integrator.

93. A method according to Claim 92,  
wherein:

5 the integrator has an output voltage level;  
the step of converting the analog signals to  
digital signals further includes the steps of

10 i) applying the second reference voltage  
level to a first input of a comparator, and  
ii) applying the output voltage level of the  
integrator to a second input of the comparator;

15 the comparator has a first output voltage  
level when the voltage level applied to the first  
input of the comparator is less than the voltage level  
applied to the second input of the comparator, and the  
comparator has a second output voltage level when the  
20 voltage level applied to the first input of the  
comparator is greater than the voltage level applied  
to the second input of the comparator, and

the step of converting the analog signals to  
digital signals further includes the step of (iii)  
counting the number of times the comparator has the  
first output voltage level during a defined period of  
25 time.

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-165-

- 1           94. A battery pack comprising:  
terminal means for connecting the battery  
pack to a battery powered device and to a battery  
recharger;
- 5           a battery including at least one  
rechargeable battery cell connected to the terminal  
means, said battery having
- 10           i) a discharge mode for supplying  
electrical power to the battery powered device, and  
ii) a charge mode for receiving electrical  
power from the terminal means;
- 15           sensing means for sensing and generating  
analog signals representing battery voltage, battery  
temperature, and battery current;
- 20           an analog-to-digital converter for receiving  
said analog signals and converting said analog signals  
to digital signals representing battery voltage,  
battery temperature, and battery current;
- 25           a processor connected to the analog-to-  
digital converter for receiving the digital signals  
therefrom, and for performing predefined calculations  
using said digital signals, wherein said predefined  
calculations include calculating an actual full  
capacity of the battery at predefined times; and
- 30           a memory area for storing data values  
including at least values representing battery  
voltage, battery temperature and battery current.
- 35           95. A battery pack according to Claim 94,  
wherein:

-166-

1           the battery has charge-discharge cycles, in  
each of said cycles, the battery is charged and  
discharged;

5           the processor includes means to identify the  
ends of at least selected ones of the charge-discharge  
cycles; and

10           the processor calculates the actual  
full capacity of the battery at the ends of at least  
selected ones of the charge-discharge cycles.

96. A battery pack according to Claim 95,  
wherein:

the processor maintains

15           i) an uncertainty value representing an  
uncertainty in the full capacity of the battery, and  
ii) a nominal full capacity value

representing a nominal full capacity of the battery;  
after each identified end of one of the  
charge-discharge cycles, if the uncertainty value is  
20           less than a given percentage of the nominal full  
capacity value, then the processor calculates the  
actual full capacity of the battery.

97. A battery pack according to Claim 95,  
wherein:

25           the processor further includes

i) means to determine a correction value,  
and

30           ii) means to determine the capacity of the  
battery at the ends of the charge-discharge cycles;  
and

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-167-

1           at the end of a given charge-discharge  
cycle, when the processor calculates a new value for  
the actual full capacity value of the battery, the  
processor calculates said new value according to the  
5 equation

$$nCAP_{FC} = oCAP_{FC} + (oCAP_{FC})x - CAP_{REM}$$

where:  $nCAP_{FC}$  is the new value for the actual full  
capacity of the battery,  
 $oCAP_{FC}$  is the most recently previously  
10 calculated value for the actual full  
capacity of the battery,  
 $x$  is the correction value determined by the  
processor, and  
15  $CAP_{REM}$  is the capacity of the battery at the  
end of the given charge-discharge cycle.

98. A battery pack according to Claim 97,  
wherein the means to determine the correction value  
includes means to determine the correction value based  
20 on battery temperature and battery current.

99. A battery pack according to Claim 98,  
wherein the means to determine the correction value  
includes:  
25 a look-up table having a multitude of stored  
values; and

means to select one of said stored values  
based on the battery temperature and battery current.

100. A battery pack according to Claim 96,  
wherein the predefined calculations further include  
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-168-

1 calculating the uncertainty value at predetermined  
times.

101. A battery pack according to Claim 100,  
wherein the uncertainty value is reset to zero at  
5 given times.

102. A battery pack according to Claim 101,  
wherein:

each charge-discharge cycle has a charging  
portion and a discharging portion;

10 the processor includes means to detect a  
plurality of predefined end of charge conditions  
during the charging portion of each charge-discharge  
cycle, and to terminate the charging portion of the  
charge-discharge cycle when one of said end of charge  
15 conditions is detected; and

the processor resets the uncertainty value  
to zero when one of said end of charge conditions is  
detected.

20 103. A battery pack according to Claim 102,  
wherein:

each charge-discharge cycle has a charging  
portion and a discharging portion;

25 the processor includes means to detect a  
plurality of predefined end of discharge conditions  
during the discharging portion of each charge-  
discharge cycle, and to terminate the discharging  
portion of the charge-discharge cycle when one of said  
30 end of discharge conditions is detected; and

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-169-

1           the processor resets the uncertainty value  
to zero when one of said end of discharge conditions  
is detected.

5           104. A battery pack according to Claim 101,  
wherein:

each of the charge-discharge cycles has a  
charging portion and a discharging portion;

10           the processor includes means to determine  
the accumulated amount of current conducted to the  
battery during the charging portion of each charge-  
discharge cycle; and

15           when the uncertainty value is calculated  
during the charging portion of one of the charge-  
discharge cycles, the calculated uncertainty value is  
based on the accumulated amount of current conducted  
to the battery during the charging portion of said one  
charge-discharge cycle.

20           105. A battery according to Claim 101,  
wherein:

each of the charge-discharge cycles has a  
charging portion and a discharging portion;

25           the processor includes means to determine  
the accumulated amount of current discharged from the  
battery during the discharging portion of each charge-  
discharge cycle; and

30           when the uncertainty value is calculated  
during the discharging portion of one of the charge-  
discharge cycles, the calculated uncertainty value is  
based on the accumulated amount of current discharged

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-170-

1 from the battery during the discharge portion of said one charge-discharge cycle.

106. A method of operating a battery system having a rechargeable battery, a processor and a  
5 memory area, the method comprising:

connecting the rechargeable battery to a battery powered device to supply electrical power thereto;

10 sensing, and generating analog signals representing, battery voltage, battery temperature and battery current;

converting said analog signals to digital signals representing battery voltage, battery  
15 temperature and battery current;

storing data values in the memory area, said stored data values including at least values representing battery voltage, battery temperature and battery current; and

20 the processor performing predefined calculations using said digital signals, including the step of calculating actual full capacity of the battery at predetermined times.

107. A method according to Claim 106,  
25 wherein:

the battery has charge-discharge cycles, in each of said cycles, the battery is charged and discharged;

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-171-

1 the method further comprises the step of  
identifying the ends of at least selected ones of the  
charge-discharge cycles; and

5 the step of calculating the actual full  
capacity of the battery includes the step of  
calculating the actual full capacity of the battery at  
the ends of at least selected ones of the charge-  
discharge cycles.

10 108. A method according to Claim 107,  
wherein:

the step of performing predefined  
calculations further includes the steps of the  
processor

15 i) maintaining an uncertainty value  
representing an uncertainty in the full capacity of  
the battery, and

20 ii) maintaining a nominal full capacity  
value representing a nominal full capacity of the  
battery; and

the step of calculating the actual full  
capacity of the battery includes the step of, after  
each identified end of one of the charge-discharge  
cycles, calculating the actual full capacity of the  
25 battery if the uncertainty value is less than a given  
percentage of the nominal full capacity value.

109. A method according to Claim 106,  
wherein:

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-172-

- 1           the step of performing predefined  
calculations further includes the step of determining  
a correction value; and
- 5           the step of calculating the actual full  
capacity of the battery includes the step of  
calculating a new value for the actual full  
capacity of the battery according to the equation
- $$nCAP_{N} = oCAP_{P} + (oCAP_{P})x - CAP_{REF}$$
- 10       where  $nCAP_{N}$  is the new value for the actual full  
capacity of the battery,  
 $oCAP_{P}$  is the most recently previously  
calculated value for the actual full  
capacity of the battery,
- 15        $x$  is the determined correction value, and  
 $CAP_{REF}$  is the capacity of the battery at the  
time said new value is calculated.
110. A method according to Claim 109,  
wherein the step of determining the correction value
- 20 includes the step of determining the correction value  
based on battery temperature and battery current.
111. A method according to Claim 110,  
wherein the memory area includes a look-up table  
having a multitude of stored values, and wherein the
- 25 step of determining the correction value includes the  
step of selecting one of the values from the look-up  
table on the basis of the battery temperature and the  
battery current.
112. A method according to Claim 109,
- 30 wherein the step of determining the uncertainty value
- 35

-173-

1 includes the step of calculating the uncertainty value  
at predefined times

113. A method according to Claim 112,  
wherein the step of determining the uncertainty value  
5 further includes the step of resetting the uncertainty  
value to zero at given times.

114. A method according to Claim 113,  
wherein:

10 the method further includes the steps of  
i) charging the rechargeable battery  
during each charge-discharge cycle,

ii) discharging the rechargeable battery  
during each charge-discharge cycle, and

15 iii) during the discharging step, the  
processor detecting one of a plurality of predefined  
end of discharge conditions, and terminating the  
discharging step when said one of said end of  
discharge conditions is detected; and

20 the step of resetting the uncertainty value  
to zero includes the step of resetting the uncertainty  
value to zero when one of said end of discharge  
conditions is detected.

25 115. A method according to Claim 113,  
wherein:

the method further includes the steps of  
i) charging the rechargeable battery  
during each charge-discharge cycle, and

30 ii) discharging the rechargeable battery  
during each charge-discharge cycle; and

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-174-

1 the step of calculating the uncertainty  
value includes the steps of

5 i) determining the accumulated amount of  
charge conducted to the battery during each charging  
step, and

10 ii) when the uncertainty value is calculated  
during the charging step, calculating said uncertainty  
value on the basis of the accumulated amount of charge  
conducted to the battery during said charging step.

116. A method according to Claim 113,  
wherein:

15 the method further includes the steps of  
i) charging the rechargeable battery  
during each charge-discharge cycle, and

ii) discharging the rechargeable battery  
during each charge-discharge cycle; and

the step of calculating the uncertainty  
value includes the steps of

20 i) determining the accumulated amount of  
charge discharged from the battery during the  
discharging step, and

25 ii) when the uncertainty value is calculated  
during the discharging step, calculating said  
uncertainty value on the basis of the accumulated  
amount of charge discharged from the battery during  
said discharging step.

30 117. A battery pack comprising:

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-175-

- 1 terminal means for connecting the battery  
pack to a battery powered device and to a battery  
recharger;
- 5 a battery including at least one  
rechargeable battery cell connected to the terminal  
means, said battery having
- 10 i) a discharge mode for supplying  
electrical power to the battery powered device, and  
ii) a charge mode for receiving electrical  
power from the terminal means;
- sensing means for sensing and generating  
analog signals representing battery voltage, battery  
temperature, and battery current;
- 15 an analog-to-digital converter for receiving  
said analog signals and converting said analog signals  
to digital signals representing battery voltage,  
battery temperature, and battery current;
- 20 a memory area for storing data values  
including at least values representing battery  
voltage, battery temperature and battery current; and
- a processor connected to the analog-to-  
digital converter for receiving the digital signals  
therefrom and for performing predefined calculations
- 25 using said digital signals, the processor including
- i) means to calculate an uncertainty value,  
and
- ii) means to calculate one of said stored  
data values at defined times if the uncertainty value
- 30 is below a given level.

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-176-

1 118. A battery pack according to Claim 117,  
wherein the means to calculate one of said stored data  
values calculates said one of said stored data values  
at each of said defined times if and only if at said  
5 each of said defined times the uncertainty value is  
below the given level.

119. A battery pack according to Claim 118,  
wherein the means to calculate the uncertainty value  
resets the uncertainty value to zero at predetermined  
10 times.

120. A method of operating a battery system  
having a rechargeable battery, a processor and a  
memory area, the method comprising:

15 connecting the rechargeable battery to a  
battery powered device to supply electrical power  
thereto;

sensing, and generating analog signals  
representing, battery voltage, battery temperature and  
20 battery current;

converting said analog signals to digital  
signals representing battery voltage, battery  
temperature and battery current;

25 storing data values in the memory area, said  
stored data values including at least values  
representing battery voltage, battery temperature and  
battery current; and

the processor performing predefined  
30 calculations using said digital signals, including the  
steps of

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-177-

- 1           i) calculating an uncertainty value, and  
          ii) calculating one of said stored data  
values at defined times if the uncertainty value is  
below a given level.

- 5           121. A method according to Claim 120,  
wherein the step of calculating one of said stored  
data values includes the step of calculating said one  
of said stored data values at each of said defined  
times if and only if at said each of said defined  
10 times the uncertainty value is below the given level.

122. A method according to Claim 120,  
wherein:

- the battery has charge-discharge cycles,  
15 each of said cycles having a discharging portion and a  
charging portion;

          in the discharging portion of each of said  
cycles, current is discharged from the battery;

- in the charging portion of each of said  
20 cycles, current is conducted to the battery; and

          the step of calculating the uncertainty  
value includes the steps of

- i) in the discharging portion of each of  
25 said cycles, calculating an uncertainty in the  
accumulated amount of current conducted from the  
battery during the discharging portion of the cycle,  
and

- ii) in the charging portion of each of said  
30 cycles, calculating an uncertainty in the accumulated

35

-178-

1 amount of current discharged from the battery during  
the discharging portion of the cycle.

123. A circuit for making a series of  
mathematical calculations, comprising:

5 means to calculate a defined value; and  
means to assess a potential inaccuracy in  
said defined value.

124. A circuit according to Claim 123,  
wherein the means to calculate the defined value  
10 includes means to calculate the defined value at  
defined times if the potential inaccuracy in said  
defined value is below a given level.

125. A method for making a series of  
mathematical calculations, comprising:

15 providing a series of values to the  
processor; and

the processor, using said series of values  
to calculate a defined value and to assess a potential  
20 inaccuracy in said defined value.

126. A method according to Claim 125,  
wherein the using step includes the step of the  
processor calculating the defined value at defined  
times if the potential inaccuracy in said defined  
25 value is below a given level.

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-179-

- 1 127. A combination portable computer-  
rechargeable battery, comprising:  
a portable computer;  
a rechargeable battery system including
- 5 i) terminal means connected to the  
portable computer,  
ii) a rechargeable battery including at  
least one rechargeable battery cell connected to the  
terminal means,
- 10 iii) sensing means for sensing, and  
generating analog signals representing, battery  
voltage, battery temperature, and battery current;  
iv) an analog-to-digital converter for
- 15 receiving said analog signals and converting said  
analog signals to digital signals representing battery  
voltage, battery temperature, and battery current,  
v) a processor connected to the analog-to-
- 20 digital converter for receiving the digital signals  
therefrom, and for performing predefined calculations  
using said digital signals to calculate values for  
defined variables,
- 25 vi) a memory area for storing data values  
including at least values representing battery  
voltage, battery temperature and battery current;  
a data bus connected to the portable
- 30 computer and the battery system to transmit data  
between the portable computer and the battery system;

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-180-

1            wherein the portable computer includes means  
for transmitting messages over the data bus to the  
processor requesting said calculated values; and

5            wherein the processor includes means for  
receiving the messages from the computer and, in  
response to receiving said messages, transmitting to  
the computer the calculated values.

128. A combination according to Claim 127,  
10           wherein all of the digital values needed by the  
processor to perform said predefined calculation are  
received by the processor from the combination of the  
analog-to-digital converter and the memory area.

129. A combination according to Claim 127,  
15           wherein the processor included means for calculating a  
predicted remaining battery life at a present rate of  
current discharge by the battery.

130. A combination according to Claim 129,  
wherein:

20           the processor further includes

i)        means to calculate a remaining capacity  
of the battery,

ii)       means to calculate a full capacity of  
the battery,

25           iii) means to calculate an adjustment  
factor,

iv)       means to calculate an uncertainty in  
the remaining capacity of the battery; and

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-181-

1 the means for calculating the predicted  
remaining battery life calculates said remaining  
battery life according to the equation:

$$5 \quad T = \frac{C_r - (C_f)(x) - C_u}{I}$$

where, T is the predicted remaining battery  
life,

C<sub>r</sub> is the calculated remaining capacity of  
the battery

10 C<sub>f</sub> is the calculated full capacity of the  
battery,

C<sub>u</sub> is the calculated uncertainty in the  
remaining capacity of the battery, and

15 I is the battery discharge current.

131. A combination according to Claim 127,  
wherein:

the means for receiving the messages from  
the computer has an abled state and a disabled state;

20 in the abled state, the receiving means is  
able to receive requests from the computer;

in the disabled state, the receiving means  
is disabled from receiving requests from the computer;

25 the processor performs said predefined  
calculations at regular periods, each of said periods  
having first and second intervals; and

30 during the first interval of each of said  
periods, the processor performs said predefined  
calculations and places the receiving means in the  
disabled state.

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-182-

1 132. A combination according to Claim 127,  
further comprising a battery re-charger connected to  
the terminal means for supplying electrical power to  
the battery; and wherein:

5 the data bus is connected to the portable  
computer, the battery system and the battery recharger  
to transmit data between the portable computer, the  
battery system and the battery recharger;

10 wherein the battery recharger includes means  
to transmit messages to the processor requesting  
identified values; and

15 the processor further includes means for  
receiving the messages from the battery recharger and,  
in response to receiving said messages from the  
battery recharger, transmitting to the battery  
recharger the identified values.

20 133. A combination according to Claim 127  
wherein one of the values stored in the memory area is  
a nominal full capacity of the battery.

134. A combination according to Claim 133,  
wherein the processor further includes means to reset  
said nominal full capacity value.

25 135. A combination according to Claim 127,  
wherein:

the battery has charge-discharge cycles,  
each of said cycles having a charging portion and a  
discharging portion; and

30 the processor includes

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-183-

- 1           i) means to detect ends of the discharging  
portions of the charge-discharge cycles, and  
          ii) means to calculate an actual full  
capacity of the battery at the detected ends of the  
5   discharging portions of the charge-discharge cycles.

136. A combination portable computer-  
rechargeable battery according to claim 127, wherein:  
the battery has a discharge mode for  
supplying electrical current to the terminal means and  
10   to the portable computer, and a charge mode for  
receiving electrical current from the terminal means;  
the processor performs a given series of  
calculations at predefined intervals; and  
15   at each of said intervals,  
i) if the battery is in the discharge mode,  
the processor determines the amount of charge supplied  
by the battery since the most recent previous one of  
said intervals, and  
20   ii) if the battery is in the charge mode,  
the processor determines the amount of charge supplied  
to the battery since the most recent previous one of  
said intervals.

137. A combination portable computer-  
25   rechargeable battery according to Claim 136, wherein:  
at each of said intervals,  
the processor determines the amount of  
current internally discharged by the battery since the  
30   most recent previous one of said intervals.

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-184-

1 138. A combination portable computer-  
rechargeable battery according to claim 137, wherein:  
said stored values further include a full  
capacity value representing a full capacity of the  
5 battery and a remaining capacity value representing  
remaining capacity of the battery;

the processor periodically resets said full  
capacity value; and

10 the processor calculates the remaining  
capacity of the battery according to the equation

$$CAP_{REM} = CAP_{FR} - \Sigma_1 - \Sigma_2 + \Sigma_3$$

where:  $CAP_{REM}$  is the remaining capacity of the  
battery,

15  $CAP_{FR}$  is the most recently reset value for  
the full capacity value,

$\Sigma_1$  is the amount of charge internally  
discharged in the battery since the full  
capacity value of the battery was most  
20 recently reset,

$\Sigma_2$  is the amount of charge discharged by the  
battery since the full capacity value was  
most recently reset, and

25  $\Sigma_3$  is a percentage of the amount of charge  
supplied to the battery since the full  
capacity was most recently reset.

139. A method of operating a combination  
portable computer-rechargeable battery system, the  
30 rechargeable battery system including at least one

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-185-

1 rechargeable battery cell, a processor and a memory area, the method comprising:

connecting the rechargeable battery to the portable computer to supply electrical power thereto;

5 sensing, and generating analog signals representing, battery voltage, battery temperature and battery current;

converting said analog signals to digital signals representing battery voltage, battery temperature and battery current;

10 storing data values in the memory area, said stored data values including at least values representing battery voltage, battery temperature and battery current;

15 the processor performing predefined calculations using said digital signals to calculate values for defined variables; and

transmitting data and messages between the portable computer and the battery system, including the steps

20 i) transmitting messages from the portable computer to the processor requesting said calculated values, and

25 ii) the processor, in response to receiving said messages, transmitting to the computer the calculated values.

140. A method according to Claim 139, wherein:

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-186-

- 1 the battery has a discharge mode for  
supplying electrical current to the terminal means and  
to the portable computer, and a charge mode for  
receiving electrical current from the terminal means;  
5 the processor performs a given series of  
calculations at predefined intervals; and  
at each of said intervals,  
i) if the battery is in the discharge mode,  
the processor determining the amount of charge  
10 supplied by the battery since the most recent previous  
one of said intervals, and  
ii) if the battery is in the charging mode,  
the processor determining the amount of charge  
15 supplied to the battery since the most recent previous  
one of said intervals.

141. A method according to Claim 139,  
wherein all of the digital values needed by the  
processor to perform said predefined calculations are  
20 received by the processor from the combination of the  
analog-to-digital converter and the memory area.

142. A method according to Claim 139,  
wherein the step of performing the predefined  
calculations includes the step of calculating a  
25 predicted remaining battery life at a present rate of  
current discharge by the battery.

143. A method according to Claim 139,  
wherein:

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-187-

1           the step of transmitting messages to the  
processor includes the step of transmitting messages  
to a receiving means on the processor;

5           said receiving means has an abled state and  
a disabled state;

          in the abled state, the receiving means is  
able to receive requests from the computer; and

10           in the disabled state, the receiving means  
is disabled from receiving requests from the computer;

          the step of performing predefined  
calculations includes the steps of

15           i) performing the predefined calculations  
at regular periods, each of said periods having first  
and second intervals, and

          ii) during the first interval of each of  
said periods, the processor performing said predefined  
calculations and placing the receiving means in the  
disabled state.

20           144. A method according to Claim 139,  
wherein:

          the combination further includes a battery  
recharger connected to the battery for supplying  
electrical power to the battery; and

25           the step of transmitting data and messages  
includes the steps of

30           i) the battery recharger transmitting  
messages to the processor requesting identified  
values, and

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-188-

1           ii) the processor, in response to receiving  
the messages from the battery recharger, transmitting  
to the battery recharger the identified values.

5           145. A method according to Claim 139,  
wherein the storing step includes the step of storing  
in the memory area a value representing nominal full  
capacity of the battery.

10           146. A method according to Claim 139,  
further including the steps of:  
discharging the battery during discharging  
cycles; and

15           the processor, (i) detecting ends of the  
discharging cycles, and (ii) calculating an actual  
full capacity of the battery at the detected ends of  
the discharging cycles.

20           147. A method according to Claim 146,  
further including the step of, at each of said  
intervals, the processor also determining the amount  
of current internally discharged by the battery since  
the most recent previous one of said intervals.

          148. A method according to Claim 147,  
wherein:

25           the step of storing data values includes the  
step of storing a full capacity value representing a  
full capacity of the battery and a remaining capacity  
value representing remaining capacity of the battery;  
the step of performing predefined  
30           calculations includes the steps of periodically

-189-

- 1 resetting the full capacity value, and periodically  
calculating the remaining capacity of the battery;  
the step of calculating the remaining  
capacity of the battery includes the step of  
5 calculating the remaining capacity of the battery  
according to the equation

$$CAP_{REM} = CAP_{FC} - E_i - E_o + E_o$$

where  $CAP_{REM}$  is the remaining capacity of the  
battery,  
10  $CAP_{FC}$  is the most recently reset value of the  
full capacity value,  
 $E_i$  is the amount of charge internally  
discharged in the battery since the full  
15 capacity value of the battery was most  
recently reset,  
 $E_o$  is the amount of charge discharged by the  
battery since the full capacity value was  
most recently reset, and  
20  $E_o$  is a percentage of the amount of charge  
supplied to the battery since the full  
capacity was most recently reset.

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-190-

- 1 149. A battery pack comprising:  
terminal means for connecting the battery  
pack to a battery powered device and to a battery  
recharger;
- 5 a battery including at least one  
rechargeable battery cell connected to the terminal  
means, the battery having
- 10 i) a discharge mode for supplying  
electrical power to the terminal means and to the  
battery powered device, and
- ii) a charge mode for receiving electrical  
power from the terminal means;
- 15 sensing means for sensing, and generating  
analog signals representing, battery voltage, battery  
temperature, and battery current;
- an integrated circuit including
- 20 i) an analog-to-digital converter for  
receiving said analog signals and converting said  
analog signals to digital signals representing battery  
voltage, battery temperature, and battery current, and
- 25 ii) a processor connected to the analog-to-  
digital converter for receiving the digital signals  
therefrom, and for performing predefined calculations  
using said digital signals,
- wherein the integrated circuit comprises a  
multitude of layers, said multitude of layers  
including upper and lower layers,
- 30 wherein said lower layers form a random  
access memory area for storing a plurality of variable

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-191-

- 1 data values, said plurality of variable data values  
including at least data values representing battery  
voltage, battery temperature and battery current, and  
wherein said upper layers form a read only  
5 memory area for storing a plurality of fixed data  
values.

150. A battery pack according to Claim 149,  
wherein the upper layers are formed using a metal  
mask.

- 10 151. A battery pack according to Claim 149,  
wherein said fixed data values include a unique  
battery identification code.

- 15 152. A battery pack according to Claim 149,  
wherein the read only memory area contains a plurality  
of fixed algorithms.

153. A battery pack according to Claim 149,  
for use by a customer having a need for a specific  
algorithm, and wherein the read only memory area  
20 stores said specific algorithm.

154. A battery pack according to Claim 149,  
wherein:

- 25 each of the upper layers includes a matrix  
consisting of  $n$  rows and  $m$  columns, the rows and  
columns intersecting to form  $n \times m$  matrix locations;  
and

a respective one transistor is located at  
each one of the matrix locations.

- 30 155. A battery pack according to Claim 154,  
wherein:

-192-

1           each of the upper layers further includes a  
plurality of common lines having a common electrical  
voltage level;

5           each of the transistors includes a source  
terminal and a drain terminal;

the source terminals of selected transistors  
are directly connected to the drain terminals of other  
transistors; and

10          both the source and drain terminals of other  
selected transistors are directly connected to one of  
the common lines.

156. A battery pack according to Claim 155,  
wherein:

15          the transistors in each of said upper layers  
consist of first and second groups of transistors;

the source terminals of the first group of  
transistors are directly connected to the drain  
terminals of others of the transistors; and

20          the source and drain terminals of the  
transistors of the second group are directly connected  
to one of the common lines.

157. A battery pack according to Claim 155,  
wherein both the source and drain terminals of each  
25          one of said other selected transistors are directly  
connected to the same one of the common lines.

158. A method of customizing a battery  
system for a specific application, the battery system  
comprising a rechargeable battery, sensing means for  
30          sensing and generating signals representing a

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-193-

- 1 plurality of battery parameters, and an integrated  
circuit including (i) an analog-to-digital converter  
for receiving said analog signals and converting the  
analog signals to digital signals, and (ii) a  
5 processor for receiving said digital signals and for  
performing predefined calculations using said digital  
signals, the method comprising:  
forming the integrated circuit from a  
multitude of layers, said multitude of layers  
10 including upper and lower layers;  
forming a random access memory area from the  
lower layers of the integrated circuit, and storing a  
plurality of variable data values in said lower  
15 layers; and  
forming a read only memory area from the  
upper layers of the integrated circuit, and storing a  
plurality of fixed data values in said upper layers.  
159. A method according to Claim 158,  
20 wherein the step of forming the integrated circuit  
includes the step of forming said upper layer by using  
a metal mask.  
160. A method according to Claim 158,  
wherein the step of storing a plurality of fixed data  
25 values in said upper layers includes the step of  
storing a unique battery identification code in said  
upper layers.  
161. A method according to Claim 158,  
30 wherein the step of forming a read only memory area

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-194-

1 from the upper layers includes the step of storing a plurality of fixed algorithms in said upper layers.

162. A method according to Claim 158, wherein the battery system is for a customer having a  
5 need for a specific algorithm, and wherein the step of forming a read only memory area includes the step of storing said specific algorithm in said upper layers.

163. A method according to Claim 158, wherein the step of forming the integrated circuit  
10 includes the steps of:

providing each of said upper layers with a matrix consisting of n rows and m columns, the rows and columns intersecting to form n x m matrix  
15 locations; and

locating a respective one transistor at each one of the matrix locations.

164. A method according to Claim 163, wherein each of the transistors includes a source  
20 terminal and a drain terminal, and the step of forming the integrated circuit further includes the steps of:

providing each of the upper layers with a plurality of common lines having a common electrical voltage level;

25 directly connecting the source terminals of selected transistors in each of the upper layers to the drain terminals of other transistors; and

30 directly connecting both the source and drain terminals of other selected transistors in each of the upper layers to one of the common lines.

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-195-

1           165. A method according to Claim 164,  
wherein the transistors in each of said upper layers  
consist of first and second groups of transistors, and  
wherein the step of forming the integrated circuit

5 further includes the steps of:

          in each of said upper layers,  
          directly connecting the source terminals of  
the first group of transistors to the drain terminals  
of others of the transistors, and  
10           directly connecting the source and drain  
terminals of the second group of transistors to one of  
the common lines.

          166. A method according to Claim 160,  
15 wherein the step of directly connecting both the  
source and drain terminals of said other selected  
transistors in each of the upper layers to one of the  
common lines includes the step of directly connecting  
the source and drain terminals of each of said other  
20 selected transistors to the same one of the common  
lines.

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-196-

- 1           167. A battery pack comprising:  
terminal means for connecting the battery  
pack to a battery powered device and to a battery  
recharger;
- 5           a battery including at least one  
rechargeable battery cell connected to the terminal  
means, said battery having
- 10           i) a discharge mode for supplying  
electrical power to the battery powered device, and  
ii) a charge mode for receiving electrical  
power from the terminal means;
- 15           sensing means for sensing and generating  
analog signals representing battery voltage, battery  
temperature, and battery current;
- 20           an analog-to-digital converter for receiving  
said analog signals and converting said analog signals  
to digital signals representing battery voltage,  
battery temperature, and battery current;
- 25           a memory area for storing data values  
including values representing battery voltage, battery  
temperature and battery current, said memory area  
including a plurality of look-up tables, each of said  
tables containing a multitude of values;
- 30           a processor connected to the analog-to-  
digital converter for receiving the digital signals  
therefrom, connected to the memory area to receive  
values therefrom, and for performing predefined  
calculations, wherein said predefined calculations  
require a plurality of values from the look-up tables;

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-197-

1 and wherein all of said required values are obtained  
from the look-up tables in the memory area.

168. A battery pack according to Claim 167,  
wherein:

5 one of the values stored in the memory area  
is a full capacity of the battery;

one of said look-up tables contains a  
multitude of residual capacity correction factors  
stored as a function of the battery discharging  
10 current and battery temperature;

one of said calculations is a calculation of  
the residual capacity of the battery; and

the residual capacity of the battery is  
calculated according to the equation:

15 
$$\text{Residual Capacity} = (\text{Full Capacity}) (x)$$

where x is based on a residual capacity  
correction factor obtained from said one of the look  
up tables.

20 169. A battery pack according to Claim 167,  
wherein:

the battery has a relative state of charge;

the battery has a self-discharge current;

one of said look-up tables contains a  
25 multitude of self-discharge currents stored as a  
function of the battery temperature and the relative  
state of charge of the battery;

one of said calculations is a calculation of  
the amount of current self-discharged by the battery  
30 over a given time period; and

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-198-

1           the amount of current self discharged by the  
battery over a given time period is calculated  
according to the equation:

$$S = I_s \Delta t,$$

5           where, S is the amount of current self-  
discharged by the battery over the given time period,  
           $\Delta t$ , is the length of the given time period,  
and

$I_s$  is the self-discharge current obtained  
10 from said one of the look-up tables.

170. A battery pack according to Claim 167,  
wherein:

          the battery has a relative state of charge  
15 and a charging current;

          one of said look-up tables contains a  
multitude of current efficiency factors stored as a  
function of battery relative state of charge and  
battery charging current;

20           one of said calculations is a calculation of  
an amount of charge added to the battery over a given  
time period;

          the amount of charge added to the battery  
over a given time period is calculated according to  
25 the equation:

$$C = I_a \Delta t$$

          where, C is the charge added to the battery,

          I is the average current supplied to the  
30 battery during the given time period,

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-199-

- 1            $\Delta t$  is the length of the given time period,  
and
- $\epsilon$  is a current efficiency factor obtained  
from said one of the look-up tables.
- 5           171. A battery pack comprising:  
terminal means for connecting the battery  
pack to a battery powered device and to a battery  
recharger;
- 10           a battery including at least one  
rechargeable battery cell connected to the terminal  
means, said battery having
- i) a discharge mode for supplying  
electrical power to the battery powered device, and
- 15           ii) a charge mode for receiving electrical  
power from the terminal means;
- sensing means for sensing and generating  
analog signals representing battery voltage, battery  
temperature, and battery current;
- 20           an analog-to-digital converter for receiving  
said analog signals and converting said analog signals  
to digital signals representing battery voltage,  
battery temperature, and battery current;
- a memory area for storing data values  
including values representing battery voltage, battery  
25           temperature and battery current, said memory area  
including a plurality of look-up tables, said  
plurality of look-up tables including
- 30           1) a first look-up table containing a  
multitude of residual capacity correction factors

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-200-

- 1 stored as a function of battery discharging current  
and battery temperature,
- ii) a second look-up table containing a  
multitude of self-discharge currents stored as a  
5 function of battery temperature and the relative state  
of charge of the battery, and
- iii) a third look-up table containing a  
multitude of current efficiency factors stored as a  
function of the relative state of charge of the  
10 battery and battery charging current; and
- a processor connected to the analog-to-  
digital converter for receiving the digital signals  
therefrom, connected to the memory area to receive  
values therefrom, and for performing predefined  
15 calculations using said digital signal and values.
172. A method of operating a battery system  
having a rechargeable battery, a processor and a  
memory area, the method comprising:
- 20 connecting the rechargeable battery to a  
battery powered device to supply electrical power  
thereto;
- sensing, and generating analog signals  
representing, battery voltage, battery temperature and  
25 battery current;
- converting said analog signals to digital  
signals representing battery voltage, battery  
temperature and battery current;
- 30 storing data values in the memory area, said  
stored data values including at least values

-201-

1 representing battery voltage, battery temperature and  
battery current;

storing additional values in a plurality of  
look-up tables in the memory area; and

5 the processor performing predefined  
calculations using said digital signals and values  
from the memory area, wherein said predefined  
calculations require a plurality of values from look-  
up tables, and all of said required values are  
10 obtained from the look-up tables in the memory area.

173. A method according to Claim 172,  
wherein:

one of the values stored in the memory area  
15 is a full capacity of the battery;

one of said look-up tables in the memory  
area contains a multitude of residual capacity  
correction factors stored as a function of the battery  
discharging current and battery temperature; and

20 the step of the processor performing  
predefined calculations includes the step of the  
processor calculating a residual capacity of the  
battery according to the equation:

Residual Capacity = (Full Capacity) (x)

25 where x is based on a residual capacity  
correction factor obtained from said one of said look-  
up tables

174. A method according to Claim 172,  
30 wherein:

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AMENDED SHEET (ARTICLE 19)

-202-

1           one of said look-up tables in the memory  
area contains a multitude of self-discharge current  
values stored as a function of the battery temperature  
and the relative state of charge of the battery, and

5           the step of the processor performing  
predefined calculations includes the step of the  
processor calculating an amount of current self-  
discharged by the battery over a given time period  
according to the equation:  $S = I_s \Delta t_s$

10           where, S is the amount of current self-  
discharged by the battery over the given time period,  
 $\Delta t_s$  is the length of the given time period,  
and

15            $I_s$  is the self-discharge current obtained  
from said one of the look-up tables.

175. A method according to Claim 172,  
wherein:

20           one of said look-up tables in the memory  
area contains a multitude of current efficiency  
factors stored as a function of battery relative state  
of charge and battery charging current; and

25           the step of the processor performing  
predefined calculations includes the step of  
calculating an amount of charge added to the battery  
over a given period according to the equation:

$$C = I_a t_e f$$

30           where, C is the charge added to the battery,  
I is the average current supplied to the  
battery during the given time period, and

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-203-

1            $\epsilon$  is a current efficiency factor obtained  
from said one of the look-up tables.

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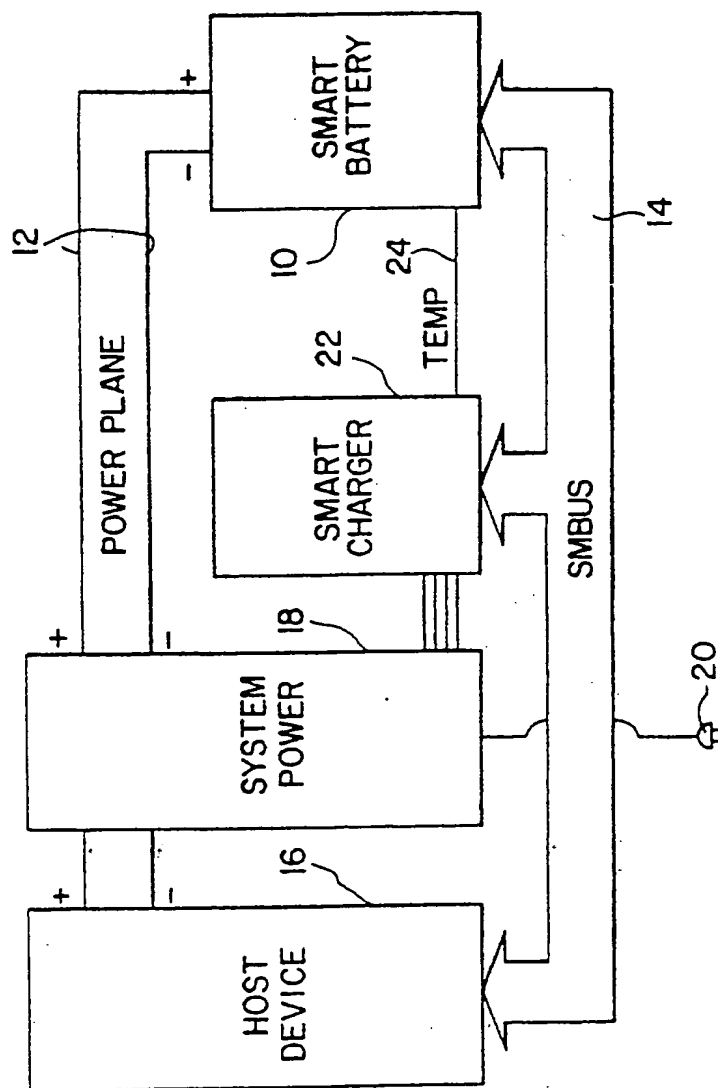
25

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1 / 31

FIG.1



2 / 31

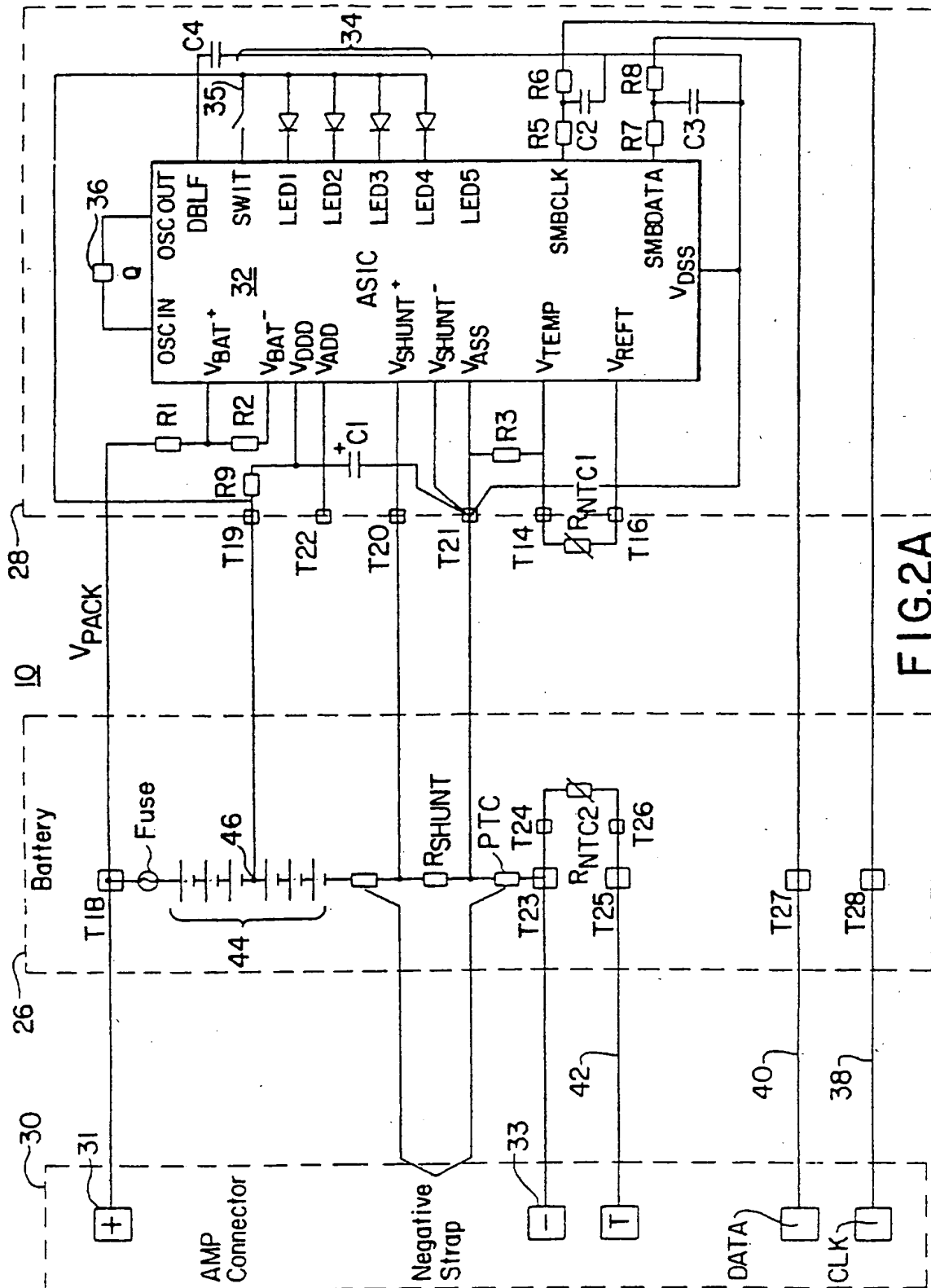
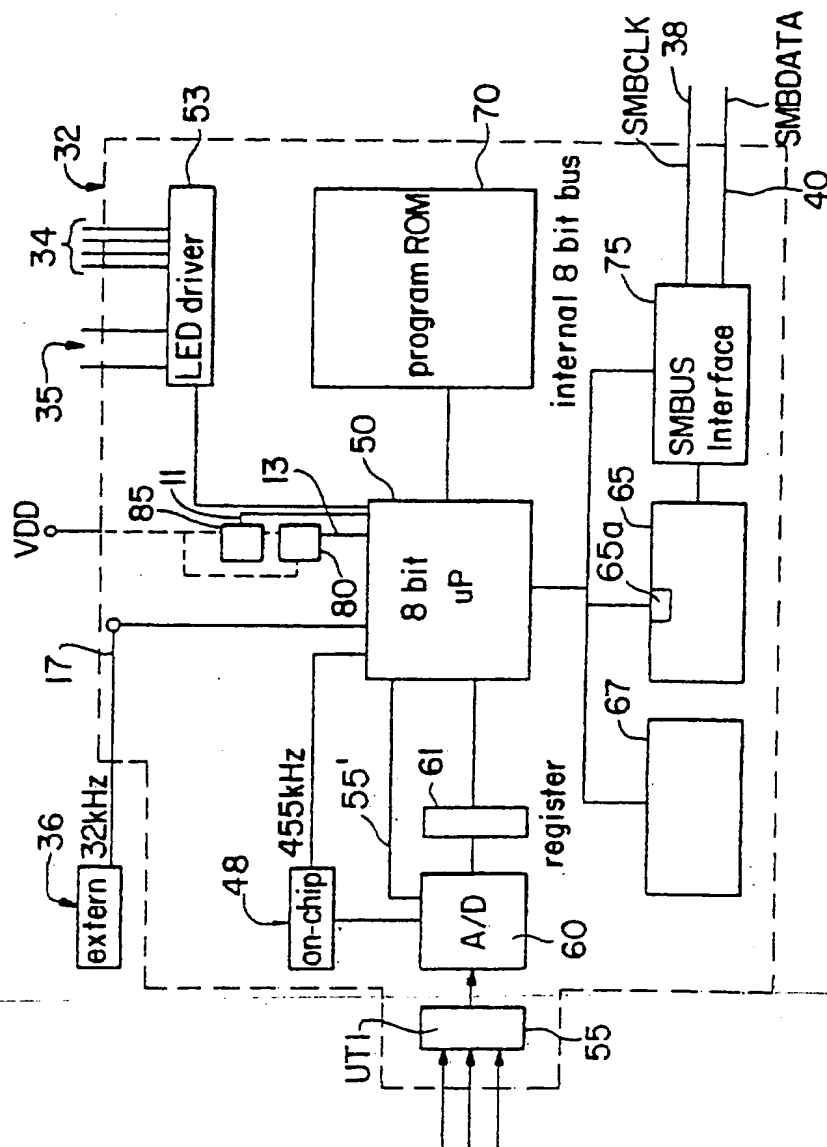


FIG. 2A

3 / 31

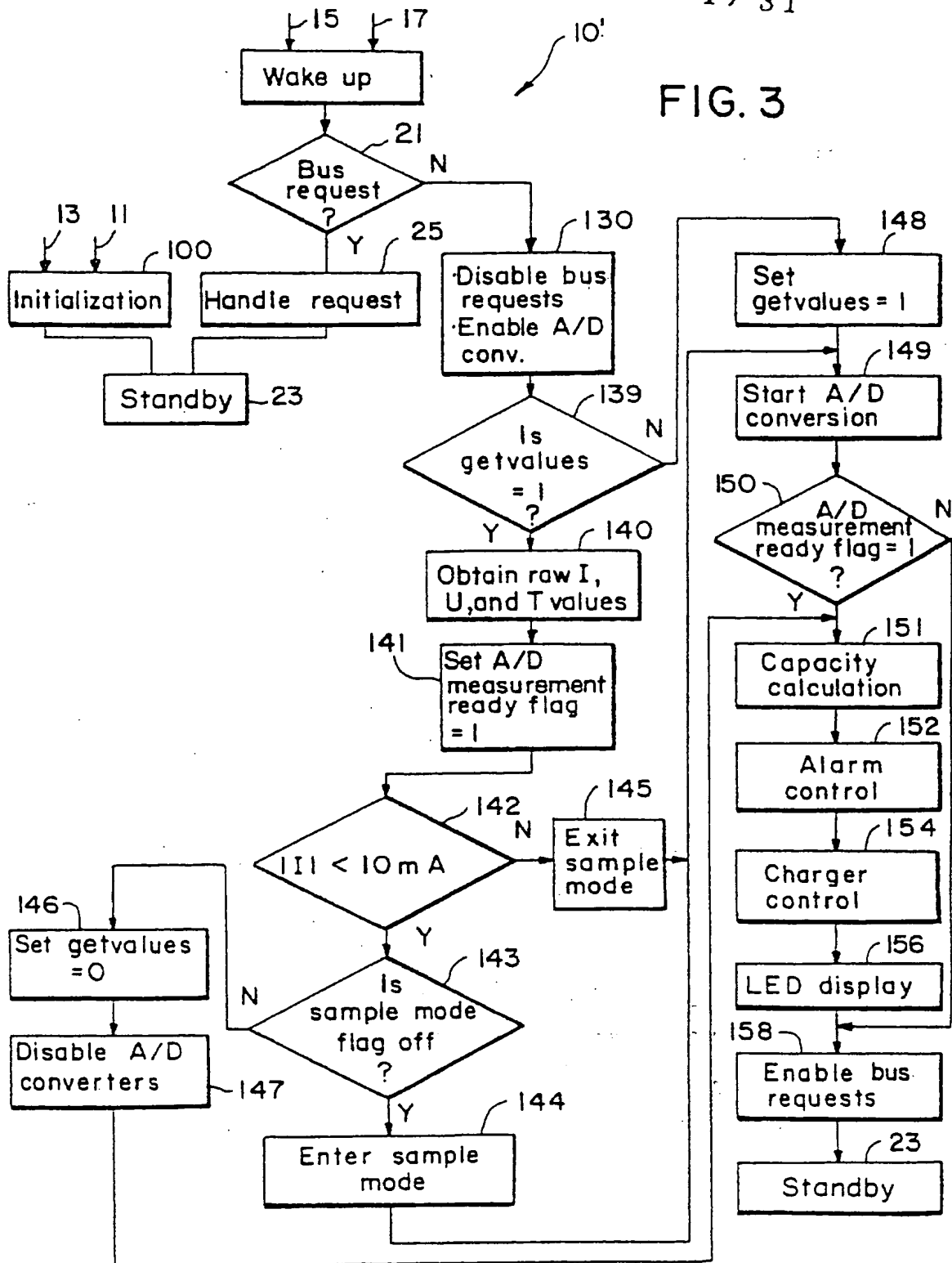
FIG.2B





4 / 31

FIG. 3



5 / 31

FIG. 4

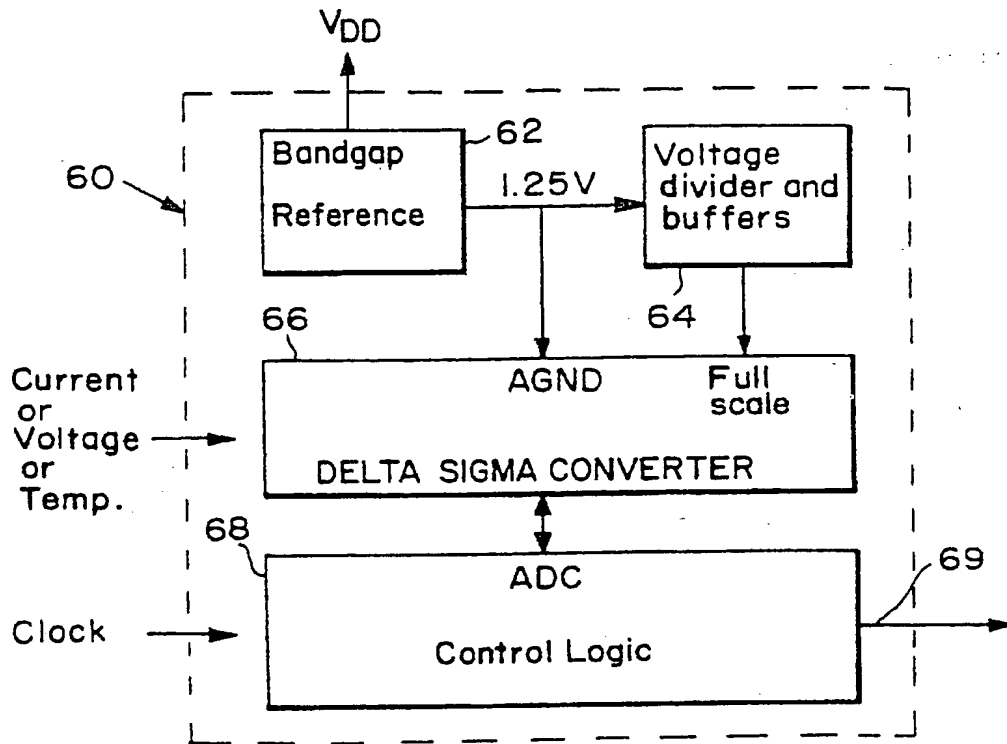


FIG. 5A

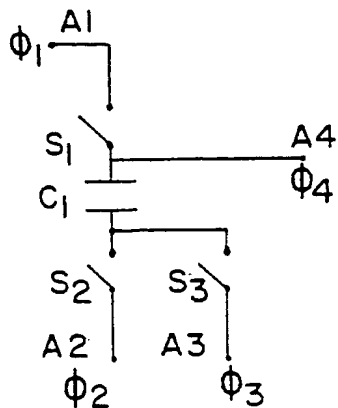
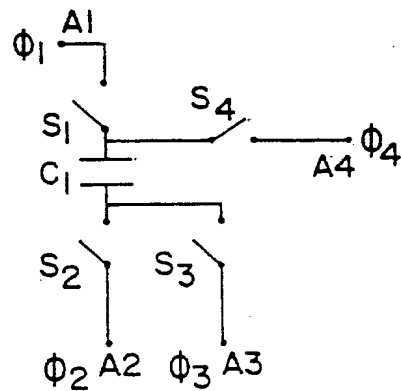


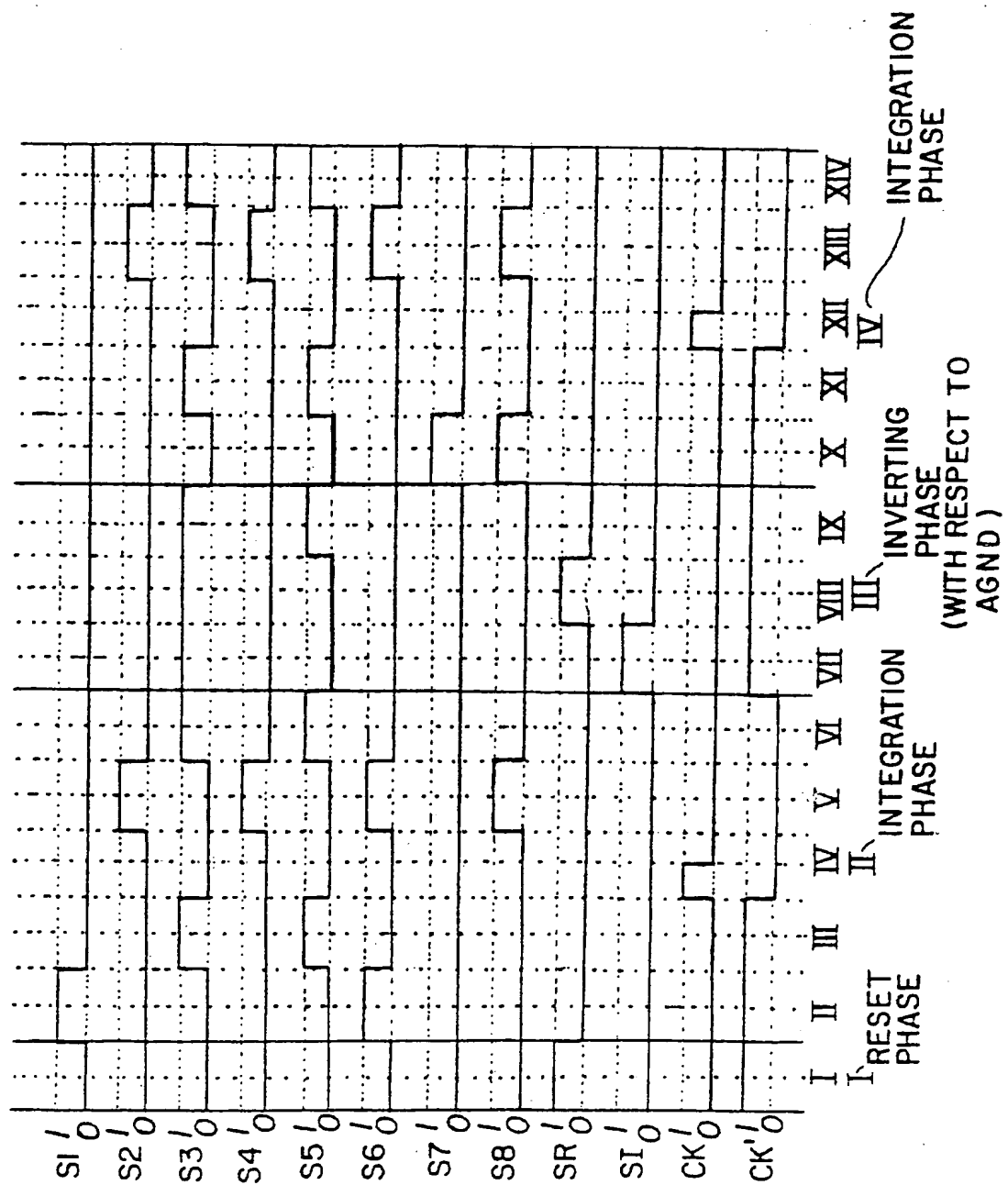
FIG. 5B



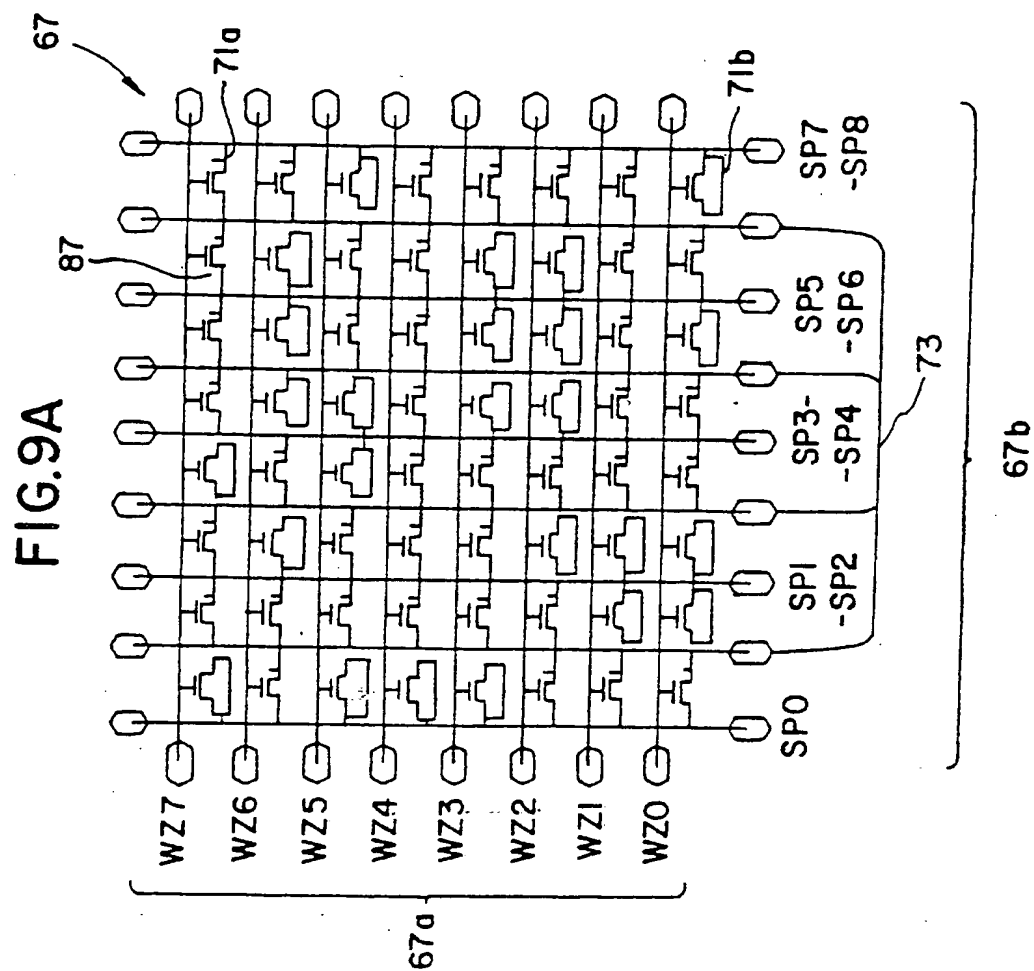


7 / 31

FIG. 7

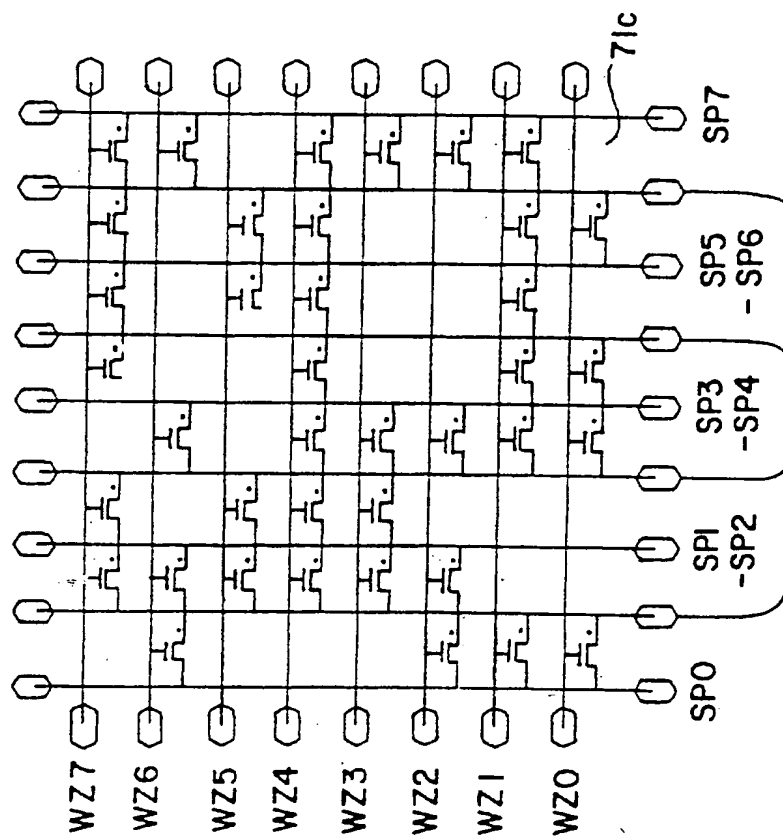






10 / 31

FIG. 9B  
PRIOR ART



11 / 31

FIG. 10

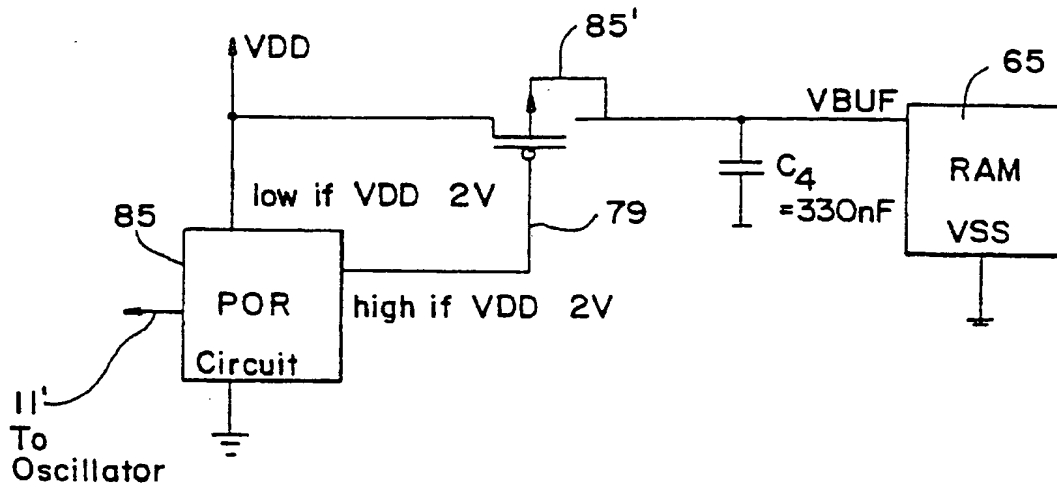
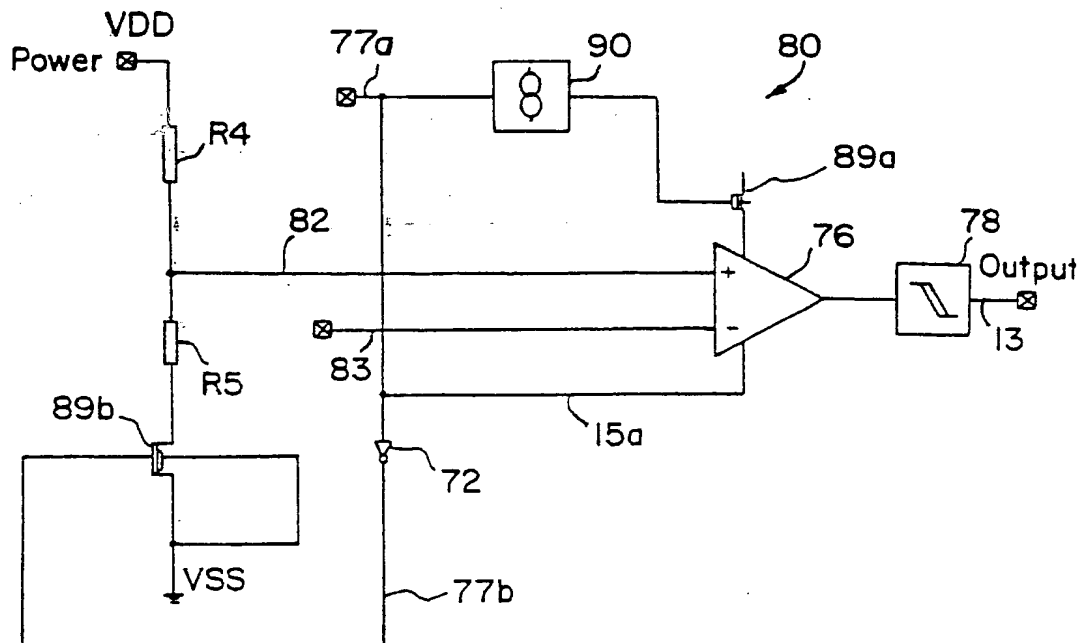


FIG. 11

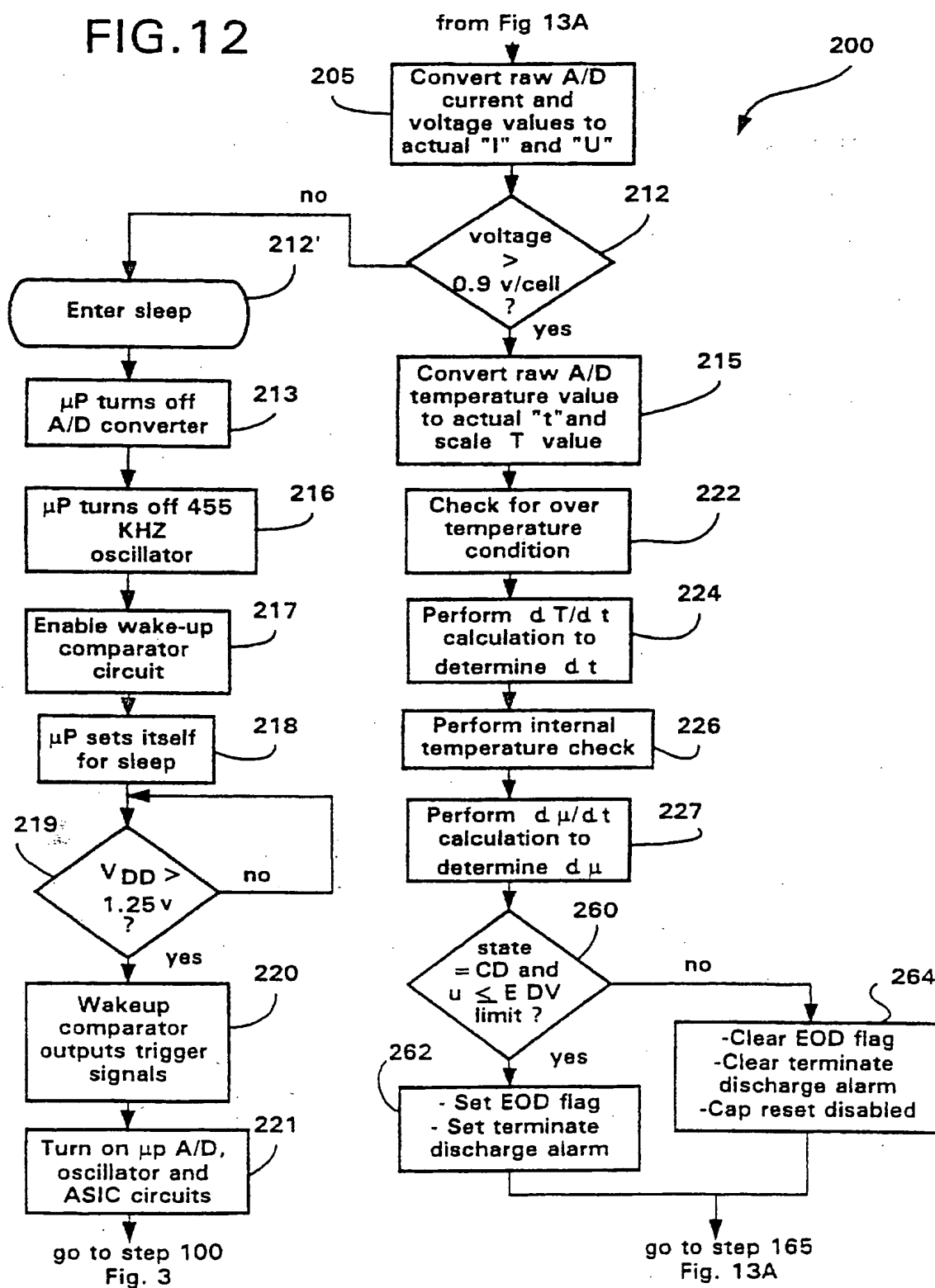


SUBSTITUTE SHEET (RULE 20)



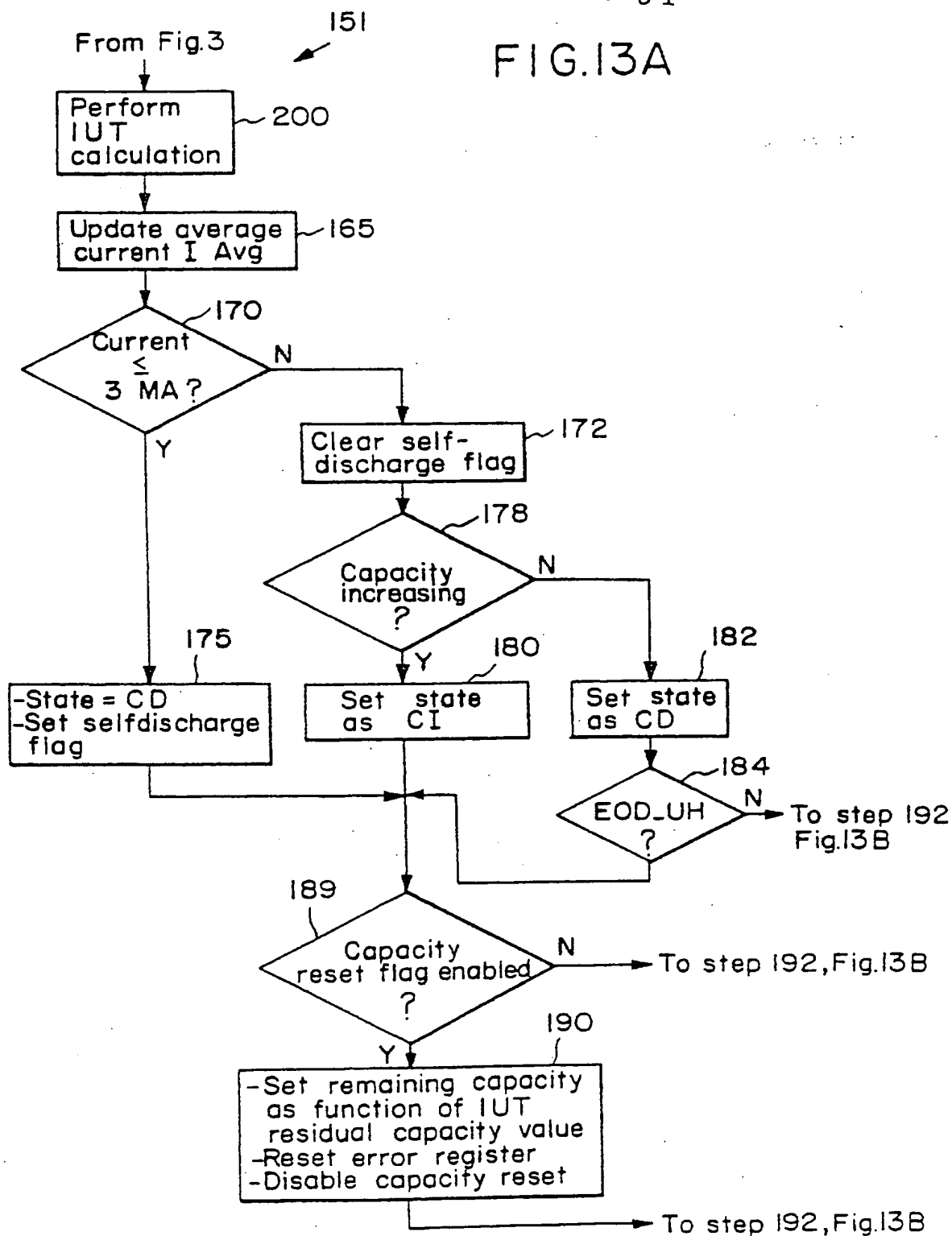
12 / 31

FIG. 12



13 / 31

FIG.13A



14 / 31

FIG. 13B

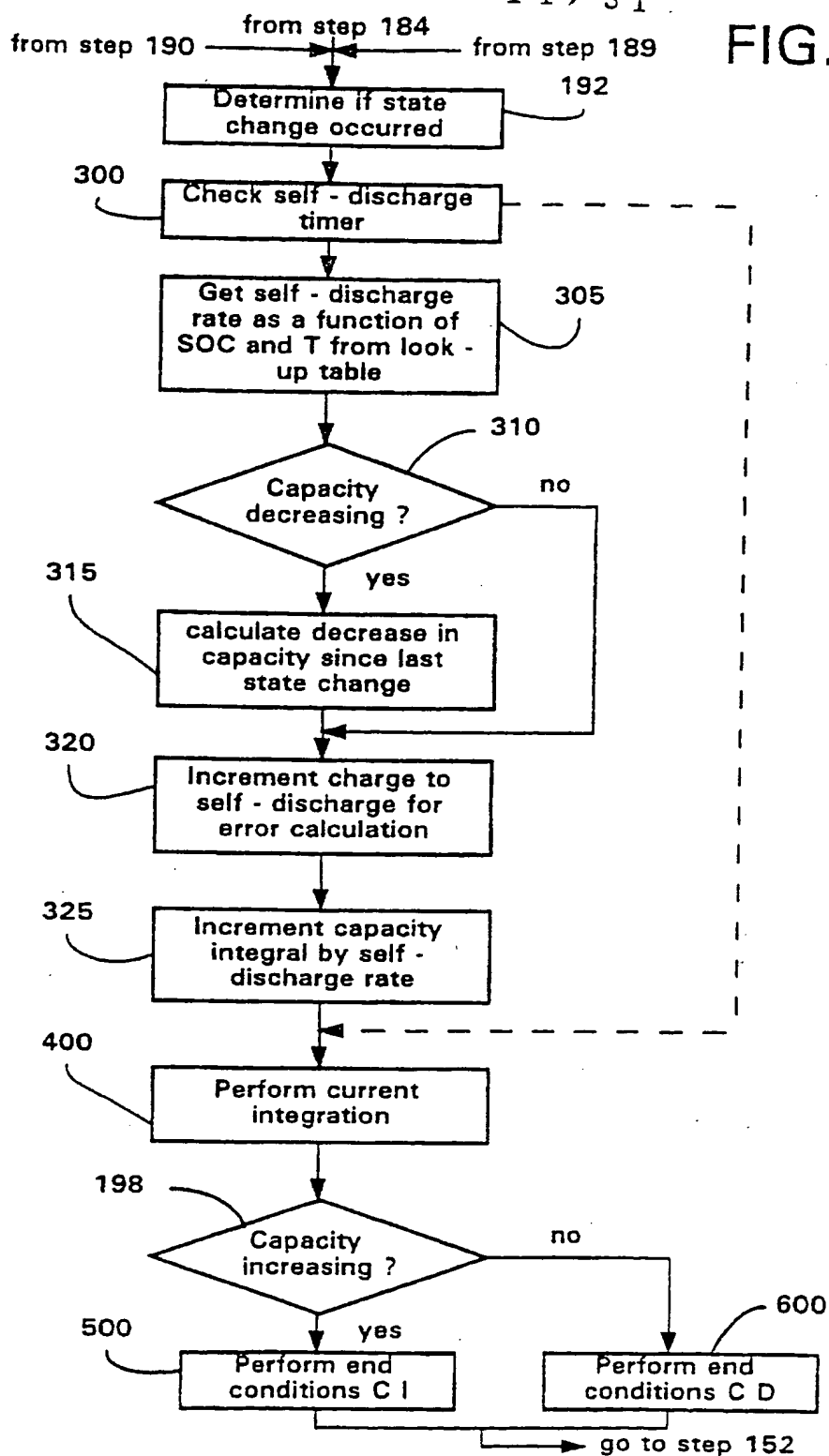


FIG 3

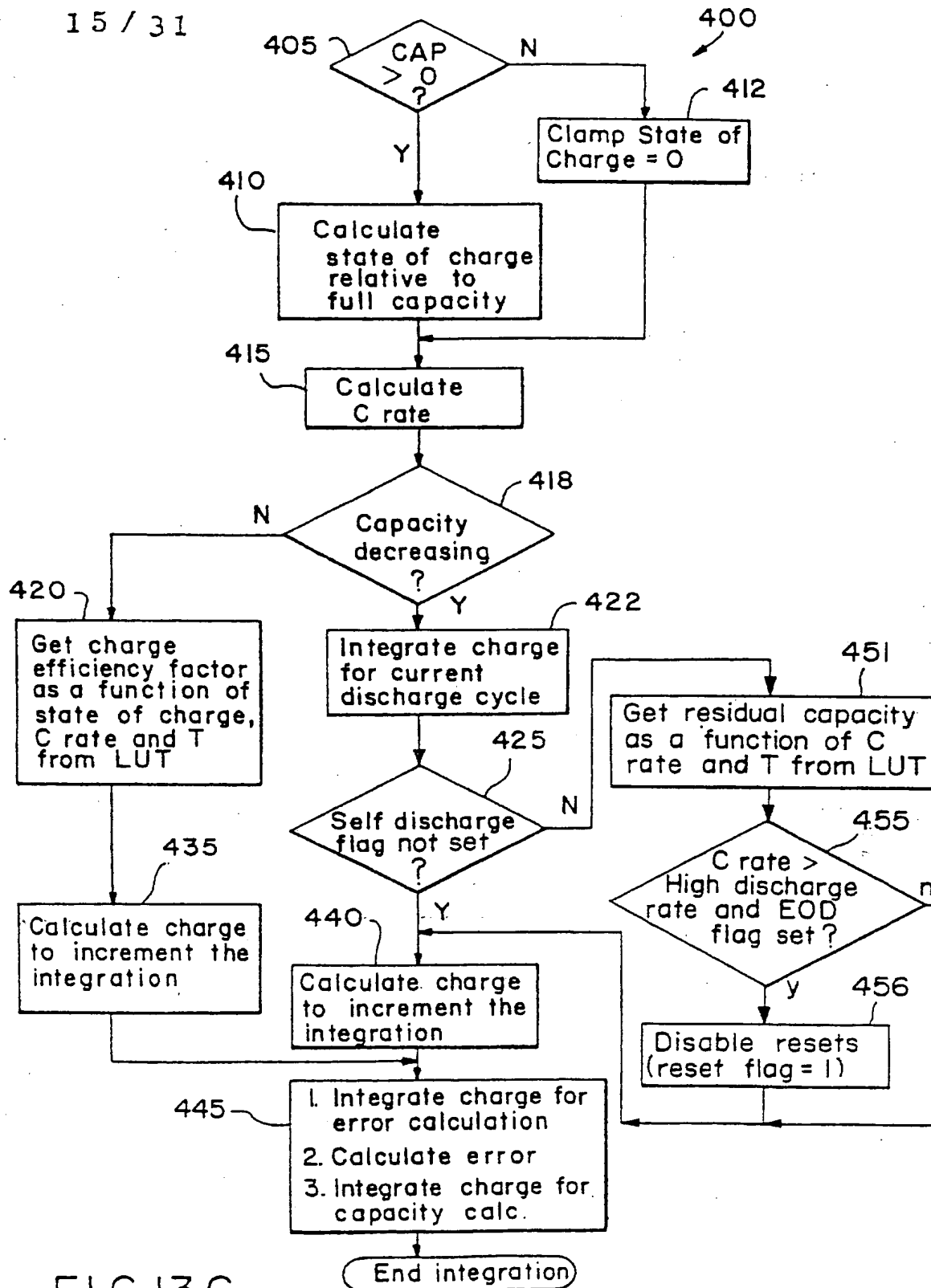
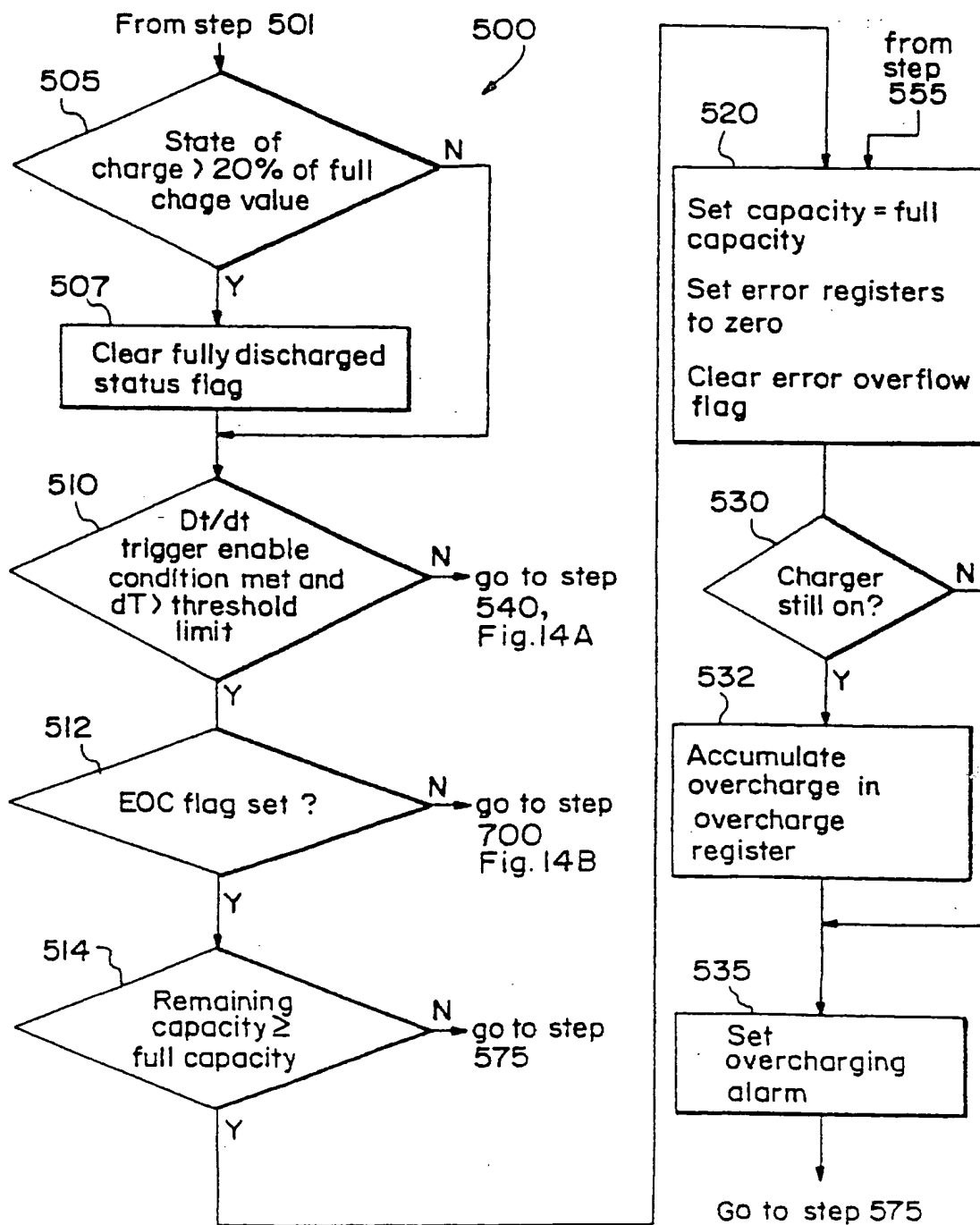


FIG.13C

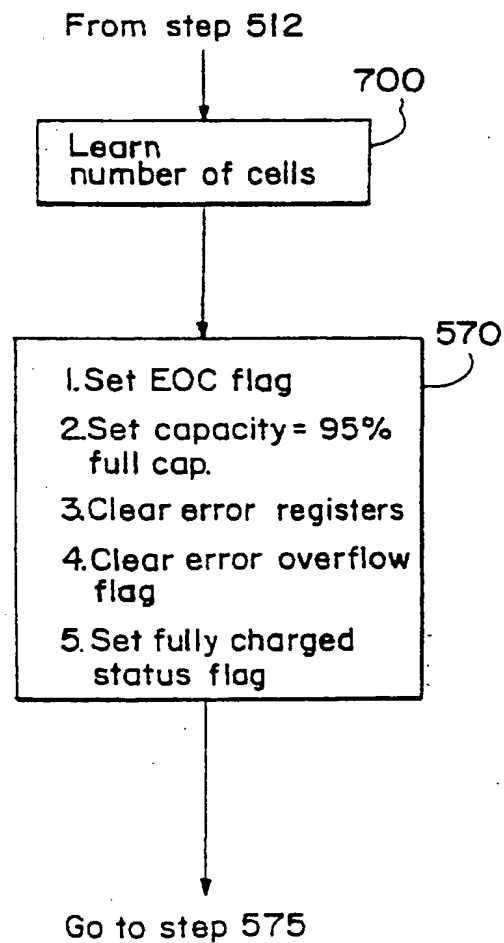
16 / 31

FIG. 14A



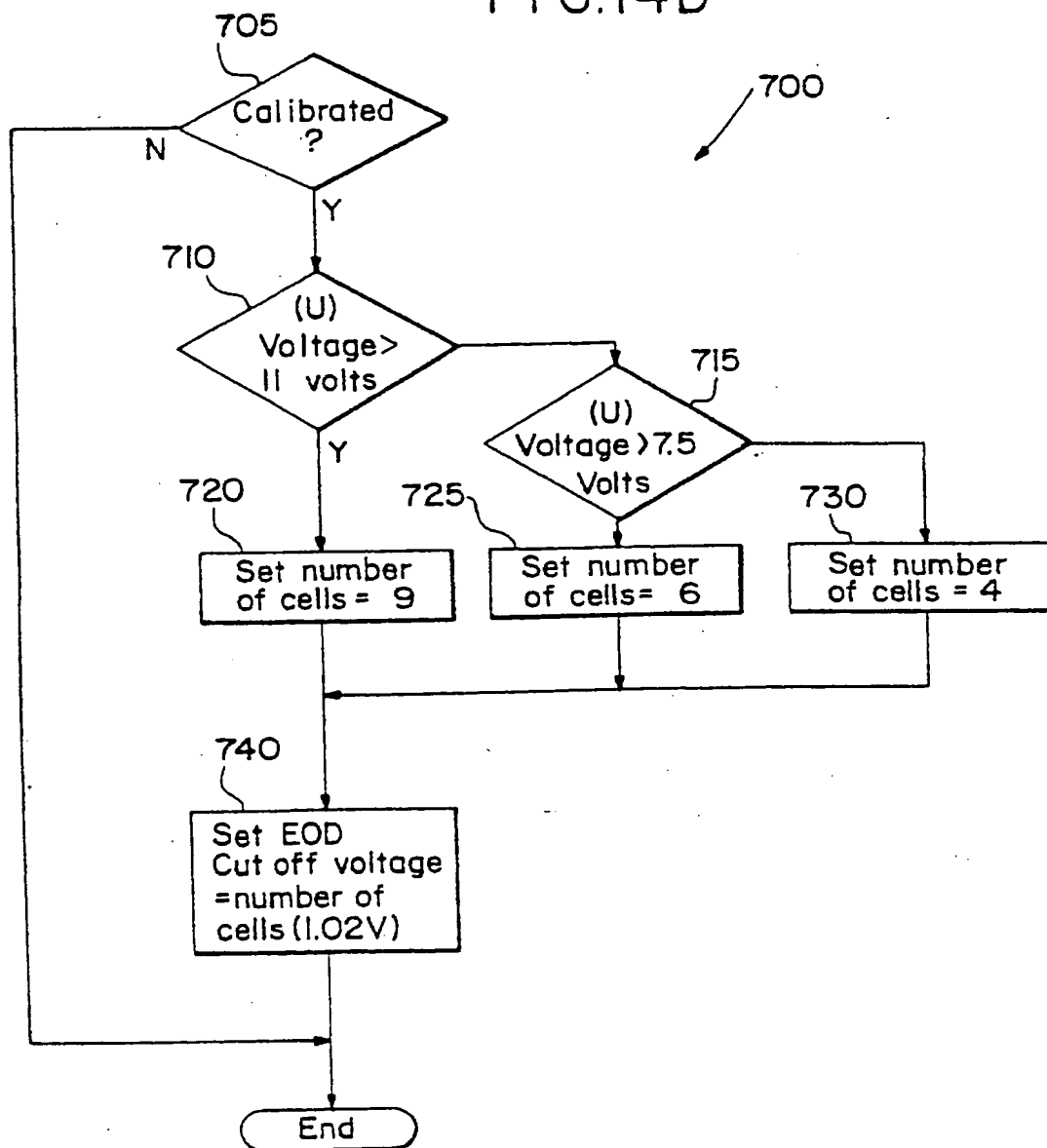
17 / 31

FIG.14B



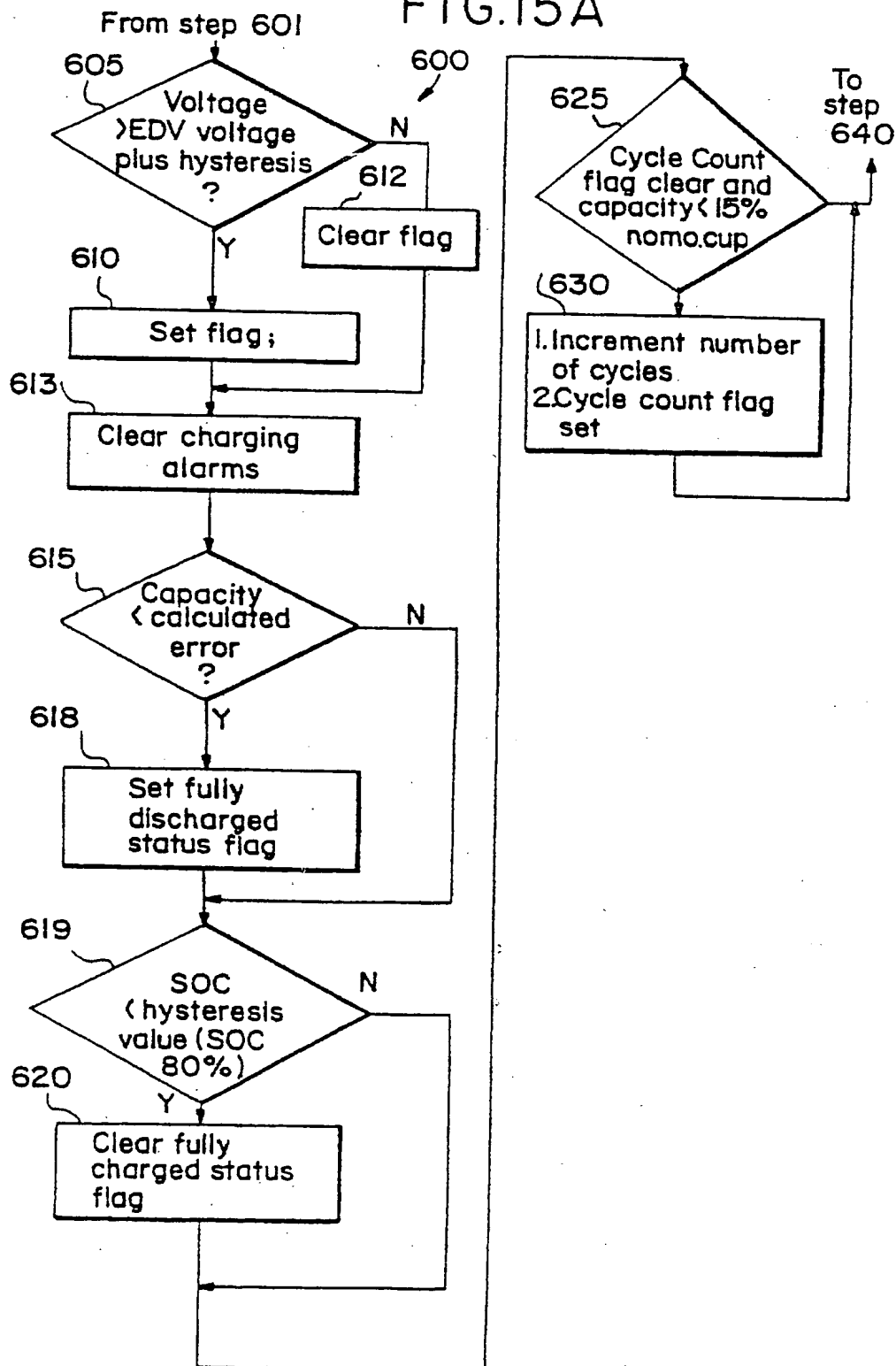
19 / 31

FIG. 14D



20 / 31

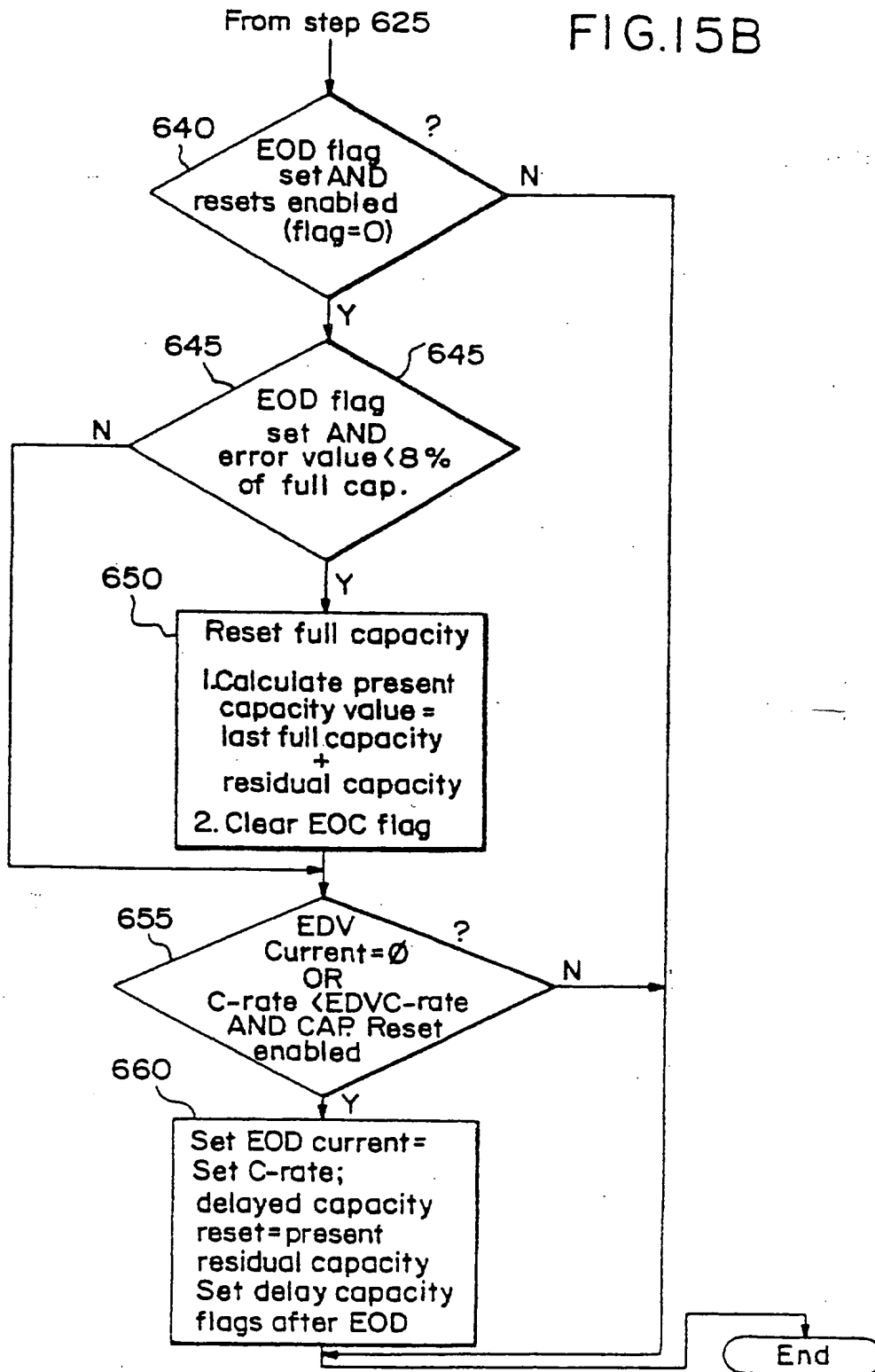
FIG.15A





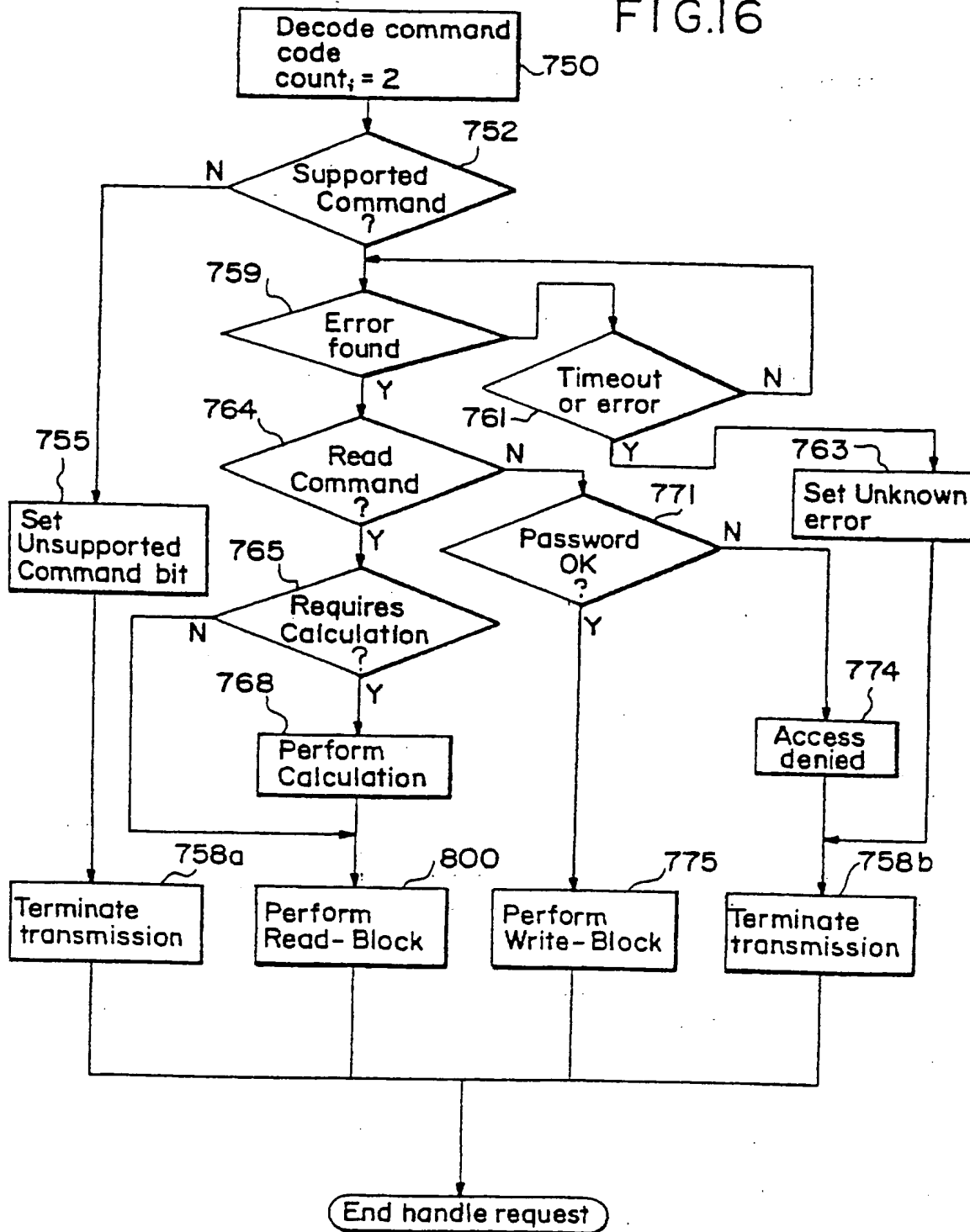
21 / 31

FIG. 15B



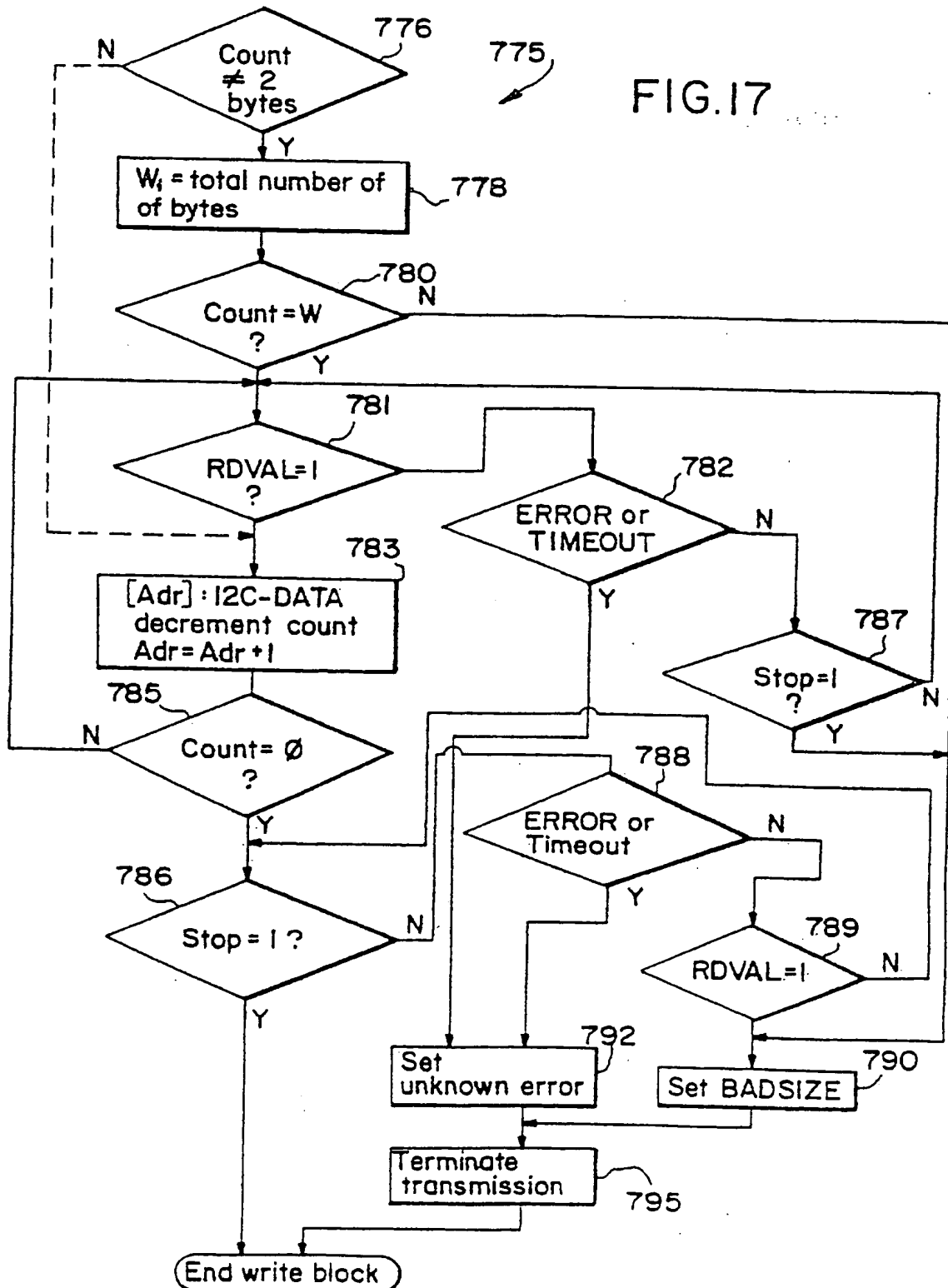
22 / 31

FIG.16



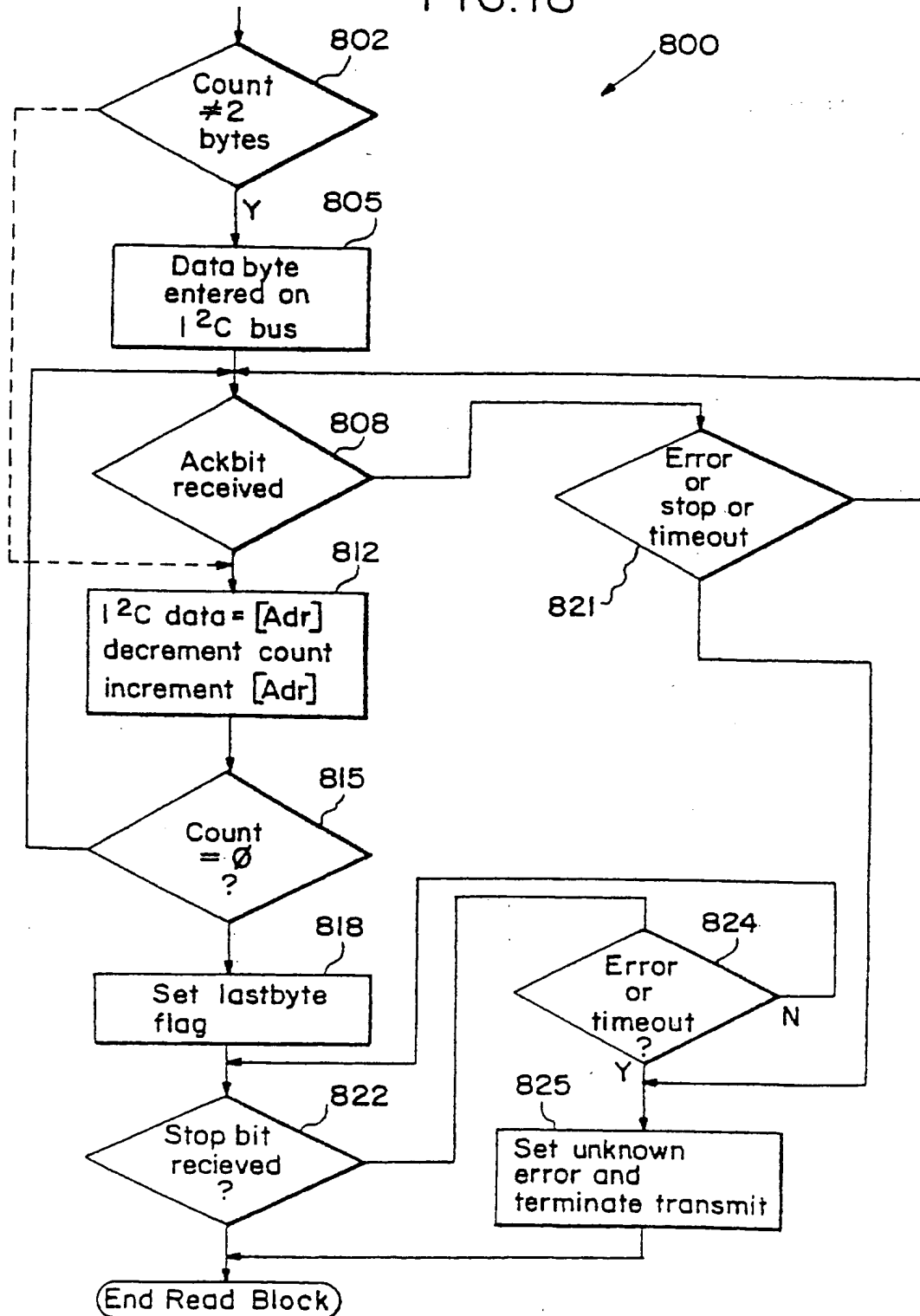
23 / 31

FIG.17



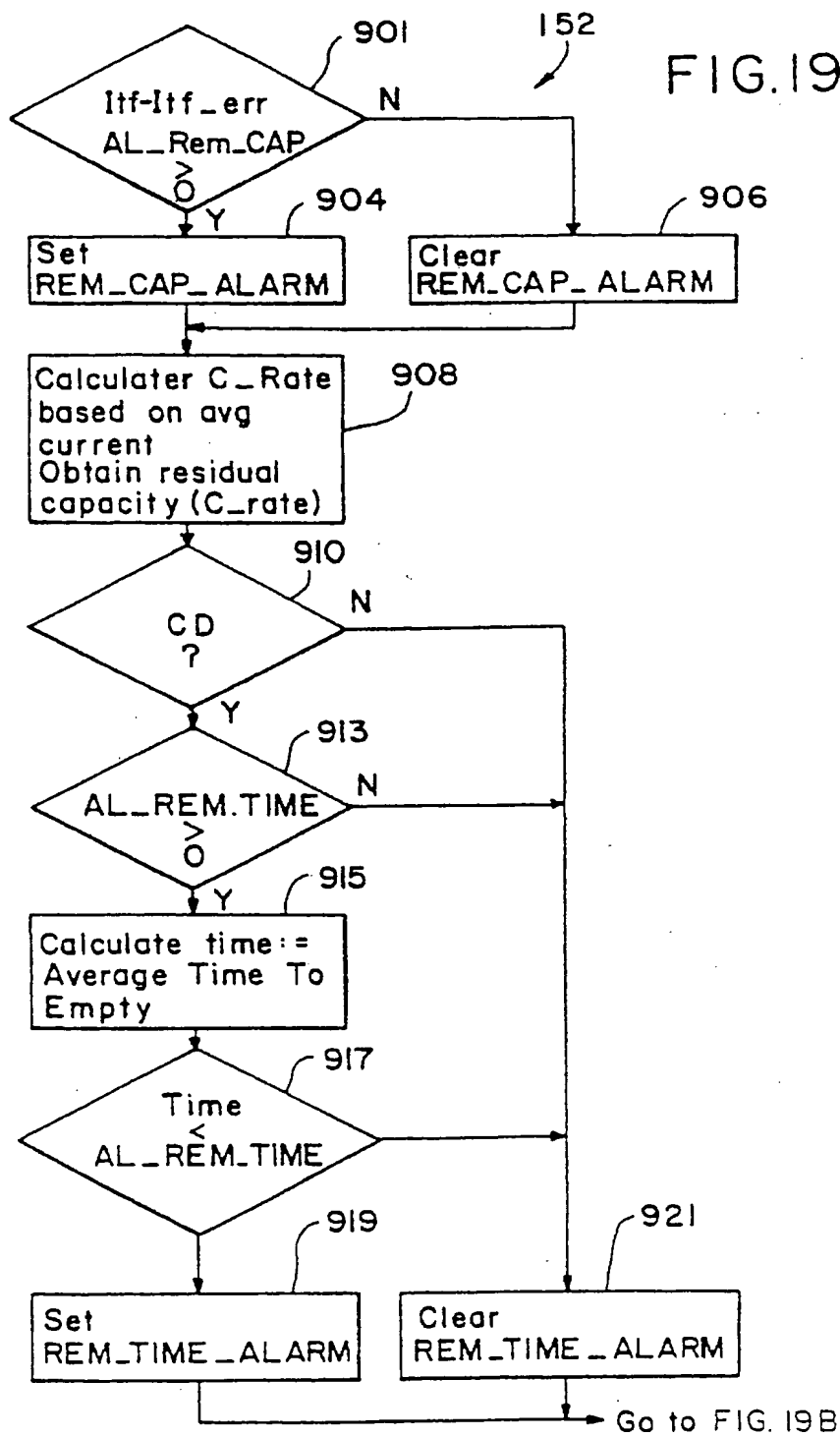
24 / 31

FIG. 18



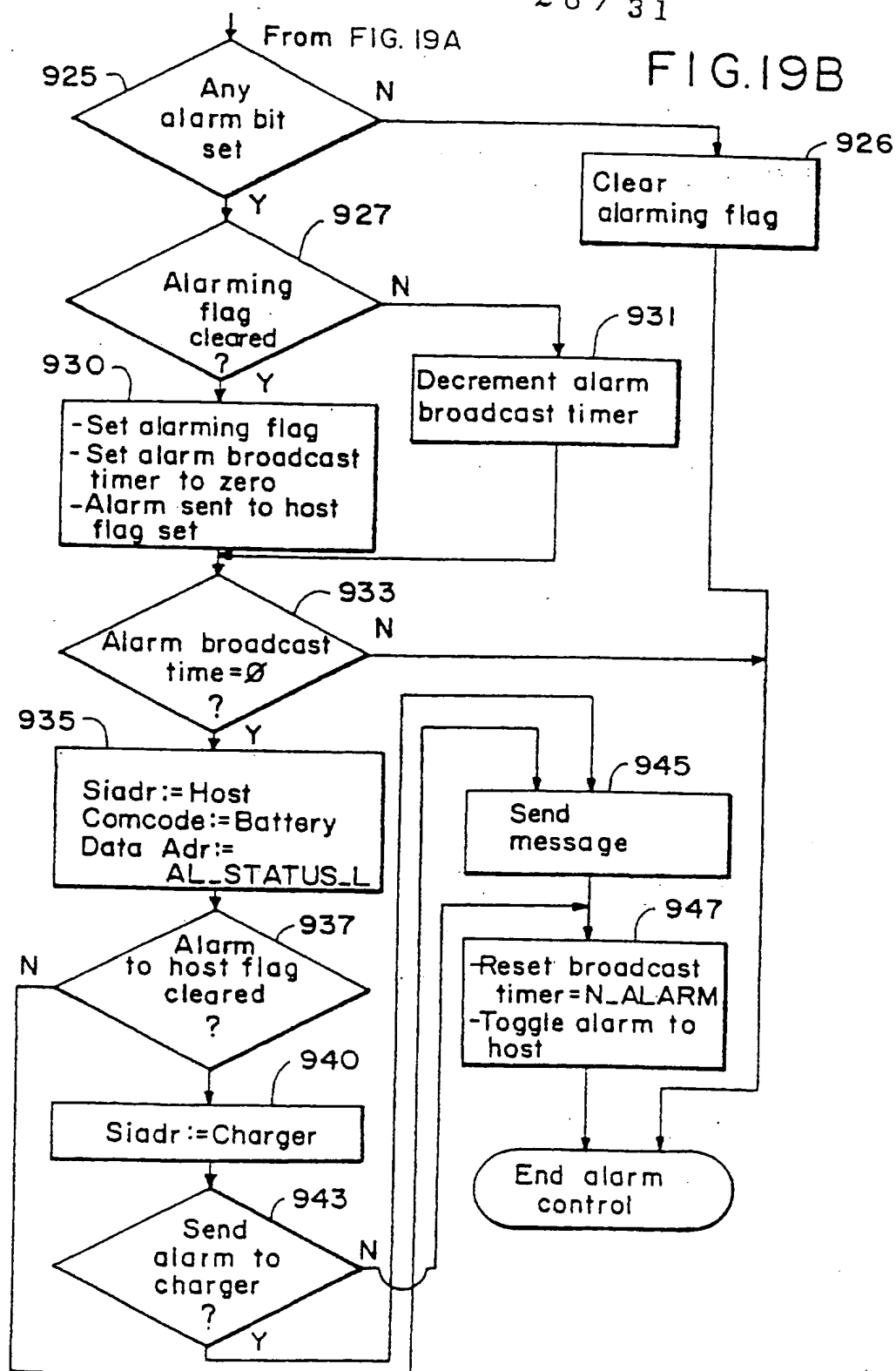
25 / 31

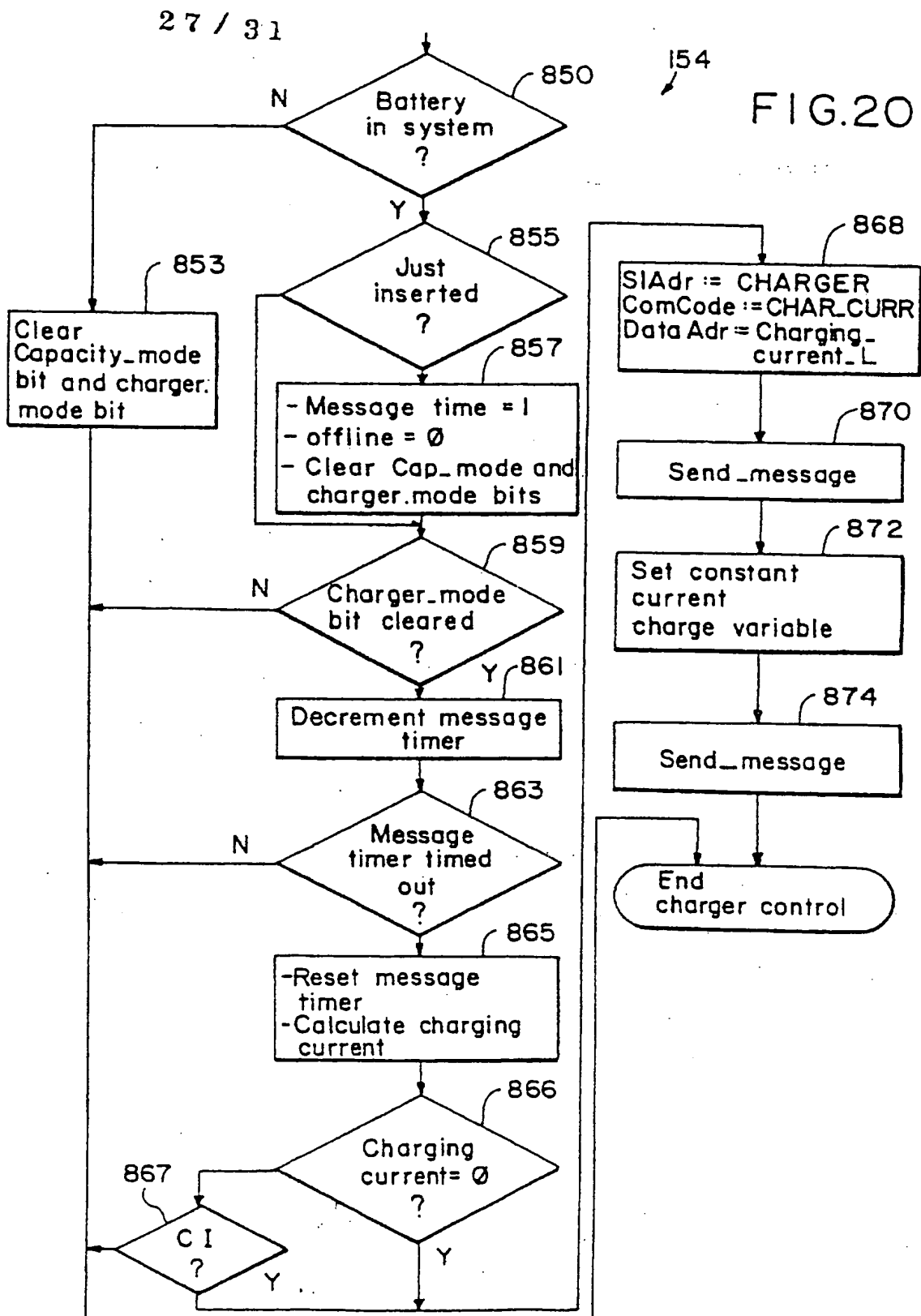
FIG. 19A



26 / 31

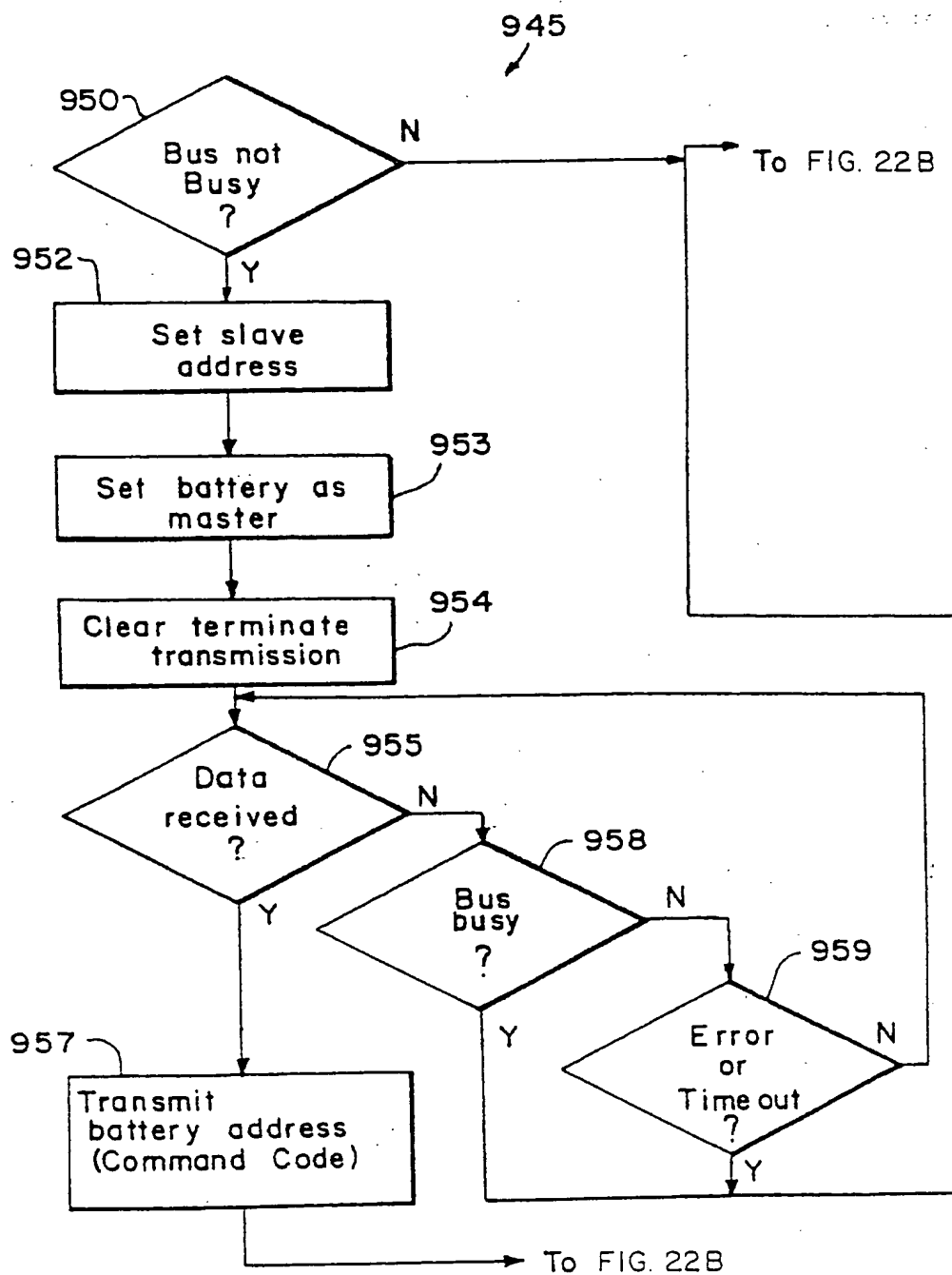
FIG. 19B





28 / 31

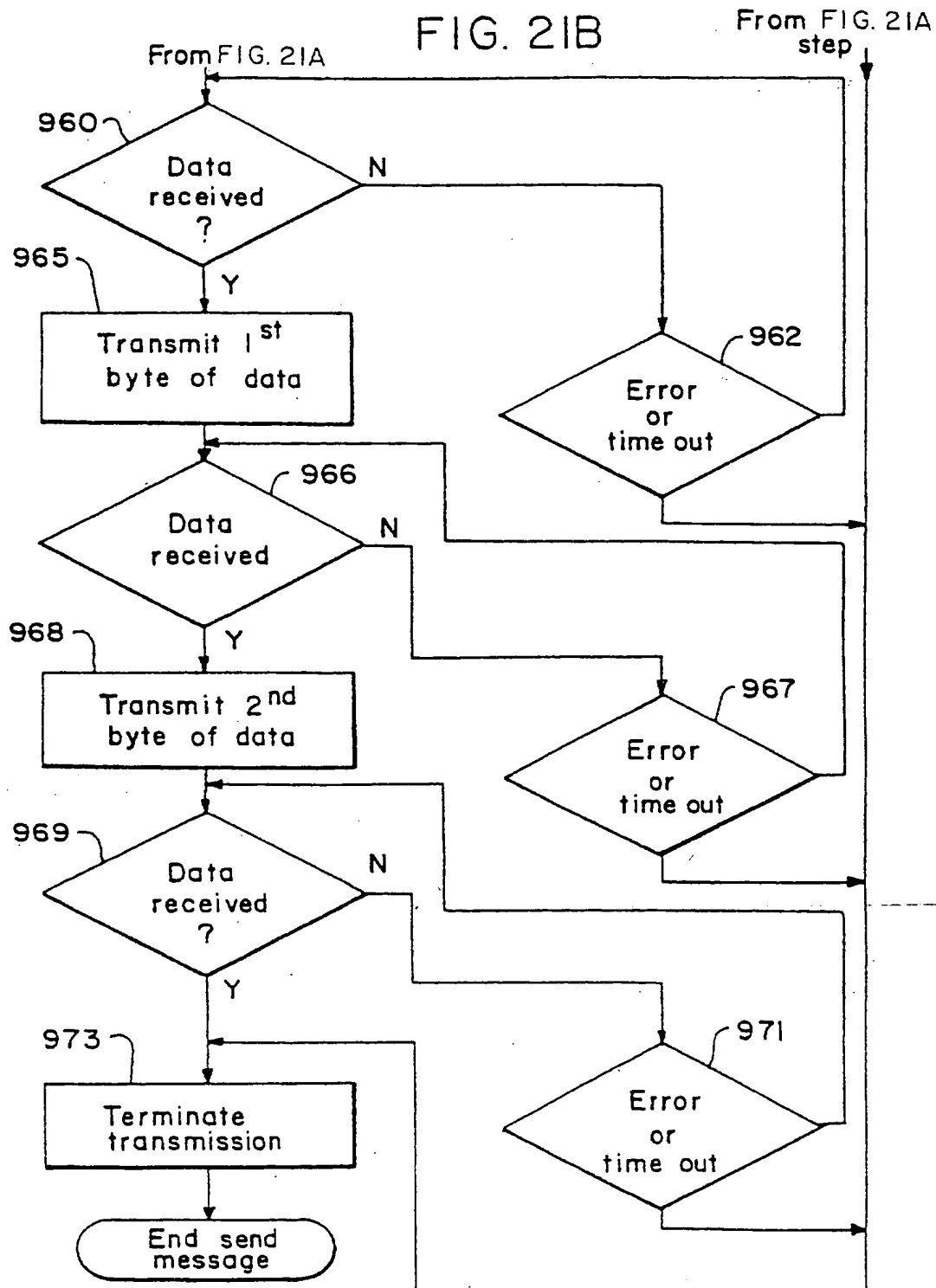
FIG. 21A





29 / 31

FIG. 21B



30 / 31

FIG. 22A

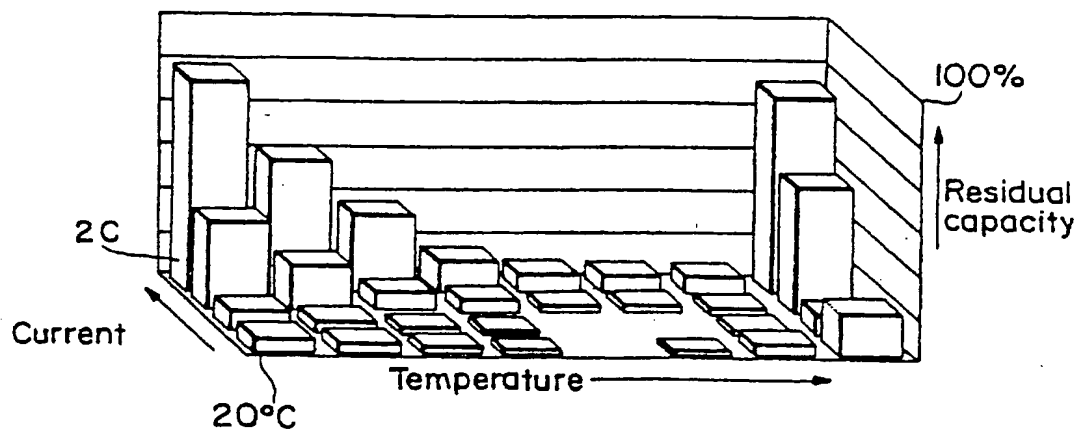
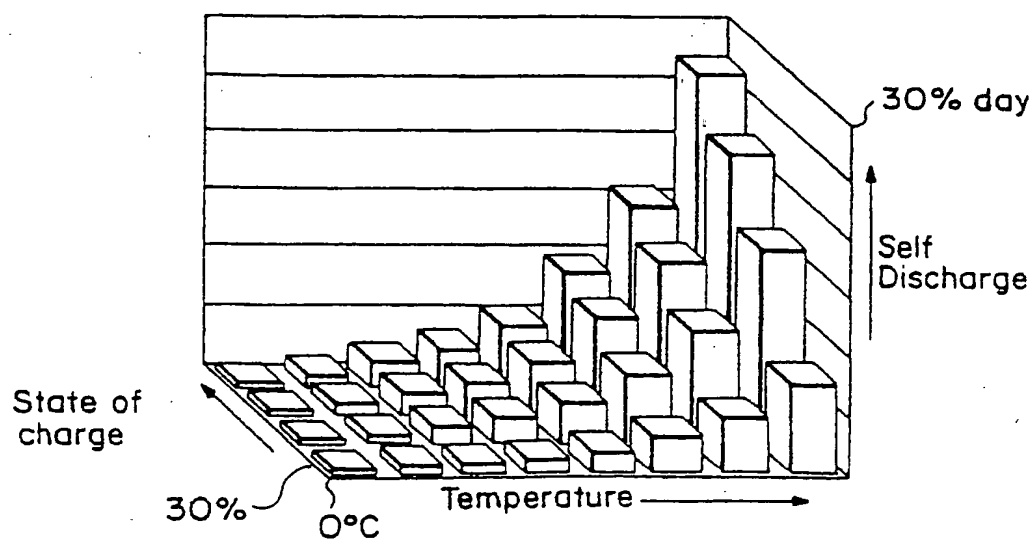


FIG. 22B



31 / 31

FIG. 22C

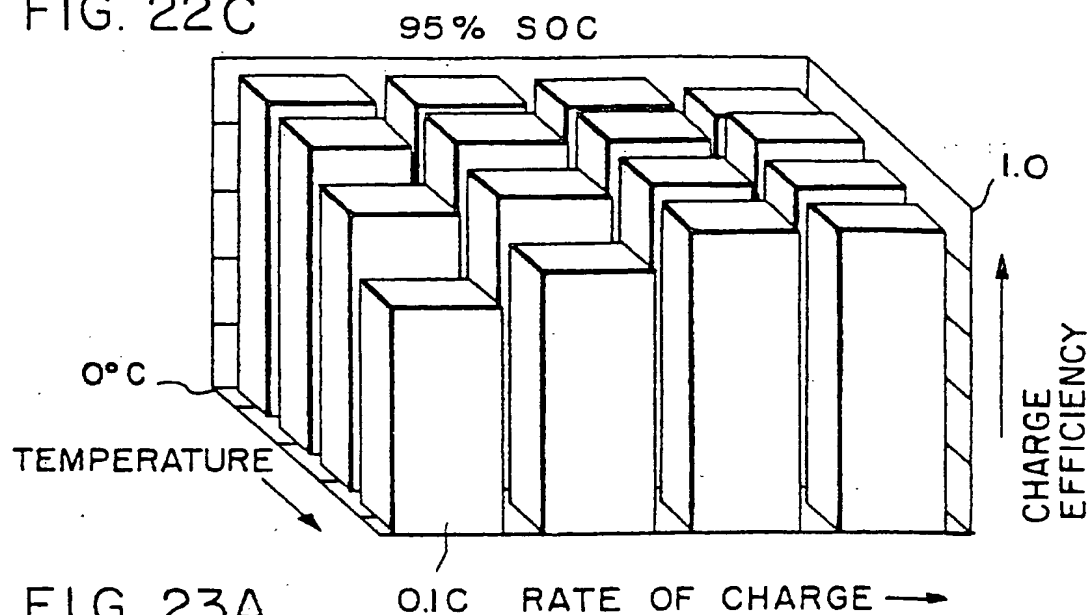


FIG. 23A

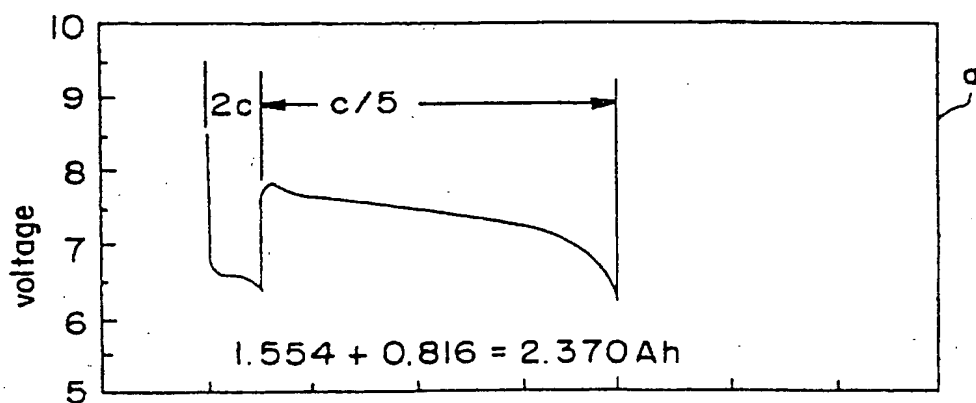
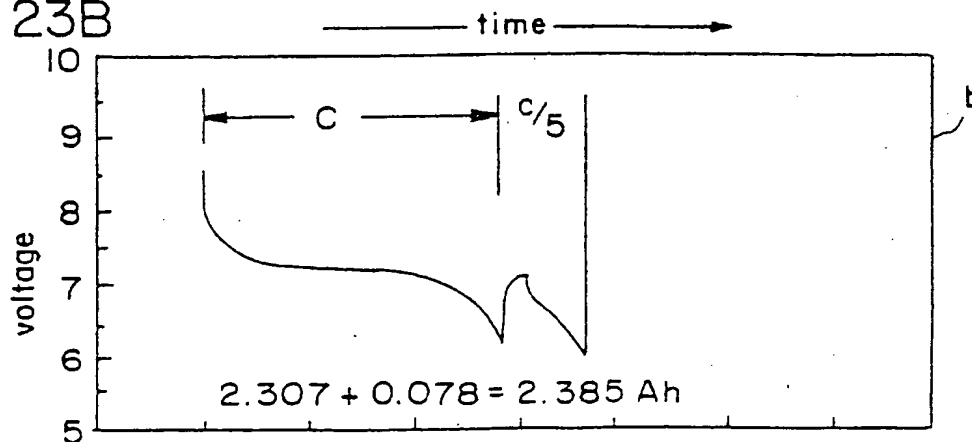


FIG. 23B



# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US95/14543

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> IPC(6) : H01M 10/44; H01J 7/04 US CL : 320/5, 11, 29, 43, 48 According to International Patent Classification (IPC) or to both national classification and IPC				
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) U.S. : Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)				
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>				
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
Y	US, A, 4,709,202 (KOENCK EL AL.) 24 November 1987, col. 5, line 1 to col. 8, line 14	1-19, 30-32, 42-45, 52		
Y	US, A, 5,345,406, (WILLIAMS) 06 September 1994, col.3 lines 1-50	21-29		
Y	US, A, 5,471,131, 28, November 1995, see the abstract	19		
A	US, A, 5,459,340, (ANDERSON ET AL.) 17 October 1995	52		
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.				
<table border="0"> <tr> <td>           * Special categories of cited documents:            "A" document defining the general state of the art which is not considered to be of particular relevance            "E" earlier document published on or after the international filing date            "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)            "O" document referring to an oral disclosure, use, exhibition or other means            "P" document published prior to the international filing date but later than the priority date claimed         </td> <td>           "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention            "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone            "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art            "&amp;" document member of the same patent family         </td> </tr> </table>			* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
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Date of the actual completion of the international search 16 JANUARY 1996		Date of mailing of the international search report <b>27 FEB 1996</b>		
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230		Authorized officer TOATLEY, GREGORY <i>Gregory Toatley</i> Telephone No. (703) 308-7889 <i>del</i>		